FLUKE ®

39/41B

Power Meter & Power Harmonics Analyzer

Service Manual

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Table of Contents

List of Tables

List of Figures

Chapter 1
Introduction and Specifications

Title	Page

1-1. Introduction

This service manual provides information on maintaining, troubleshooting, and repairing the Fluke 39 Power Meter and Fluke 41B Power Harmonics Analyzer. The information in this manual pertains to both models unless otherwise indicated. The Fluke 39 and 41B share many features and are collectively referred to as “the Tester”. “Model 41B” is mentioned when a description pertains to that model only. This manual includes the following:

- Specifications
- Theory of operation
- Calibration procedure
- Performance testing and troubleshooting procedures
- Replacement parts lists
- Schematic diagrams

A meter under warranty will be promptly repaired or replaced (at Fluke’s option) and returned at no charge. See the registration card for warranty terms. If the warranty has expired, the meter will be repaired and returned for a fixed fee. Contact the nearest Service Center for information and prices. A list of U.S. and International Service Centers is included at the end of Chapter 6 of this manual.

1-2. Organization of the Service Manual

This service manual has the following chapters.

Chapter 1. Introduction and Specifications

Chapter 1 describes the Service Manual, explains special terminology and conventions, and provides complete meter specifications.

Chapter 2. Theory of Operation

Chapter 2 treats the Tester’s circuitry as functional blocks, with a description of each block’s role in overall operation. A detailed circuit description is then given for each block. These descriptions explain operation to the component level and support the troubleshooting and repair procedures in Chapter 5.

Chapter 3. General Maintenance

Chapter 3 provides information on general maintenance, handling precautions and disassembly instructions. Instructions covering warranty repairs and shipping the instrument to a service center are also contained in this section.

Chapter 4. Performance Testing and Calibration

Chapter 4 contains information on required test equipment, performance test procedures and calibration of the instrument.

Chapter 5. Troubleshooting

Chapter 5 provides detailed repair procedures to the component level. Troubleshooting and repair procedures rely on the Theory of Operation presented in Chapter 2 and the Schematic Diagrams in Chapter 7.

Chapter 6. List of Replaceable Parts

Chapter 6 lists the parts used in the Tester as well as information on how and where to order parts.

Chapter 7. Schematic Diagrams

Chapter 7 contains the schematic diagrams for all assemblies and a list of mnemonic definitions to aid in identifying signal name abbreviations.

1-3. Conventions

The following conventions are used in this manual:

- Printed Circuit Assembly (PCA)

A “pca” is a printed circuit board and its attached parts.

- Circuit Nodes

A pin or connection on a component is specified by a dash (-) and number following the component reference designator. For example, pin 19 of U30 would be U30-19.

- User Notation

  Switch positions used in the meter circuit descriptions correspond to those in the schematic diagrams in Chapter 7.

1-4. General Information

1-5. Description

The Fluke 39 and 41B are handheld Testers used to measure voltage and current at power line and harmonic frequencies. Using these inputs, the Tester automatically calculates power and a wide range of other measurements useful in determining harmonic distortion levels and sources.

These capabilities allow you to monitor power quality before and after an installation, troubleshoot a power distribution system, and (with Model 41B) print out or download data for additional analysis.

The Tester is both a harmonics measurement tool and a power meter or digital multimeter. You can use the Tester to measure voltage events (undervoltage, overvoltage, line outages, and neutral to ground levels), current levels, or to measure power levels. Fundamental frequency measurements (to 100 Hz) and harmonic frequency measurements (to about 2 kHz) are also possible.

1-6. Power Requirements

The Tester uses 4 Alkaline “C” Cells (ANSI/NEDA-14A, IEC-LR14) for primary power. New Alkaline “C” Cells will provide a minimum of 24 hours of continuous operation (typically 48 hours). You can also use NiCad batteries; however, depending on battery condition, fully charged NiCad batteries provide 8 hours or less of continuous operation.

1-7. Options, Accessories and Related Equipment

The following accessories are supplied with the Fluke 39 and 41B:

- 80i-500s AC Current Probe
- TL-24 Test Leads (Set of two, Red and Black)
- TP-20 Test Probes (2)
- AC-20 Test Clips (2)

The following additional accessories are supplied with the Fluke 41B:

- RS-232 Cable
- 9-Pin to 25-Pin Adapter
- Plug Adapter
- 3.5 inch Micro-Floppy Disk (FlukeView™ 41 Software)

Optional accessories for both the Fluke 39 and 41B are as follows:

- 80i-1000s AC Current Probe
- C41s Soft Carrying Case

1-8. Operating Instructions

Operating instructions for the Fluke 39 and 41B can be found in the Users Manual (Fluke PN 942847). See How to Obtain Parts on page 6-1.

1-9. Specifications

Accuracy is specified for a period of one year after calibration.

Specifications expressed in the "±(2% + 3 digits)" format are saying that the error is a percent of reading plus a number of least significant digits. The least significant digit is the smallest value that can be displayed in a range and can be found in the resolution section of the Range and Resolution specifications table.

When a harmonic error is expressed in the "13^{th} (±(2% + 2 digits)) --- 31^{st} (±(5% + 2 digits))" form, it is indicating that there is a linear increase in error from the lower harmonic to the upper harmonic. The error can be determined as a ratio of the desired harmonic to the number of harmonics in the expression times the difference in error over the range plus the least error. For example, to find the 22^{nd} Harmonic error from the above equation:

((Desired Harmonic - Lower Harmonic) / (Upper Harmonic - Lower Harmonic)) X Error Difference + Least Error

((22 - 13) / (31 - 13)) X 3 + 2 = 3.5%

Therefore, the error for the 22^{nd} harmonic is ±(3.5% + 2 digits).

Frequency Range, Fundamental: 6-65 Hz and dc

Minimum Input Levels: 5V rms or 1A rms

Volts Measurements (True rms):

Input Range:	5.0V to 600V rms (ac + dc) 5.0V to ±933V peak
Basic Accuracy*:	
rms (ac + dc):	±(0.5% + 2 digits); 6-65 Hz
peak, dc:	±(2% + 3 digits)
** < 15V rms, add 2 digits*	
Input Impedance:	1 MΩ, balanced
Crest Factor:	> 3.0 below 300V, 1.56 @ 600V

Amps Measurements (True rms)

(1 mV/A) Isolated Input

Input Range:	1.00 mV (A) to 1400 mV rms (A) (ac + dc) 1.0 mV (A) to ±2000 mV (A) peak
Basic Accuracy:	
rms (ac + dc):	±(0.5% + 3 digits); 6-65 Hz + probe specs
peak, dc:	±(2% + 4 digits) + probe specs
Input Impedance:	1 MΩ || 47 pF
Crest Factor:	> 3.0 below 600 mV, 2.0 @ 1000 mV

Watts Measurements (Volt-Amps)

(1 mV/A) Isolated Input

Range:	0 W (VA) to 600 kW (kVA) average 0 W (VA) to 2000 kW (kVA) peak
Accuracy (ac + dc) Active W (VA):	±(1% + 4 digits) + probe specs

Harmonics Measurement Accuracy (Cursor Data)

(Harmonic Level > 5% Using Smooth ~20)

Volts:

Fundamental to 13th Harmonic:	±(2% + 2 digits)
13th to 31st Harmonic:	13th (±(2% + 2 digits)) -----31st (±(8% + 2 digits))

Amps* or Watts:

Fundamental to 13th Harmonic:	±(3% + 3 digits) + probe specs
13th to 31st Harmonic:	13th (±(3% + 3 digits) + probe specs) ----- ----- 31st (±(8% + 3 digits)+ probe specs)

** < 20A, add 3 digits*

Phase:

Fundamental:	(±2 degrees) + probe specs
2nd to 31st Harmonic:	2nd (±5 degrees) ---- 31st (±20 degrees) +probe specs

Frequency Measurement Accuracy (Fundamental, 6.0 Hz - 99.9 Hz)

6.0 Hz - 99.9 Hz:	±0.3 Hz

Other Measurement Specifications

Measurement Function	Range/Resolution	Accuracy
Input Bandwidth: (-0.5 dB)	DC, 6 Hz to 2.1 kHz	
Crest Factor (CF): (Using Smooth ∿-20):	1.00 to 5.00	±4%
Power Factor (PF):	0.00 to 1.00	±0.02
Power Factor Displacement (PFD):	0.00 to 0.29 0.30 to 0.69 0.70 to 0.89 0.90 to 1.00	Unspecified ±0.04 ±0.03 ±0.02
Phase Measurement Range:	-179 to 180 degrees	(see Phase above)
K-Factor (KF) Range (Model 41B):	1.0 to 30.0	±10%
Total Harmonic Distortion: %THD-F: %THD-R:	 0.0 to 799.9 0.0 to 99.9	 ±(0.03 × Reading + 2.0%) ±(0.03 × Reading + 2.0%)

Ranges and Resolution

AC Volts		AC Amps		Watts	
Range (PK)	Resolution	Range (PK)	Resolution	Range (PK)	Resolution
20V	0.1V	2A	0.01A	50W	1.0W
50V	0.1V	5A	0.01A	100W	1.0W
100V	0.1V	10A	0.01A	200W	1.0W
200V	0.1V	20A	0.01A	500W	1.0W
500V	1V	50A	0.1A	1 kW	0.01 kW
1 kV	1V	100A	0.1A	2 kW	0.01 kW
		200A	0.1A	5 kW	0.01 kW
		500A	1A	10 kW	0.1 kW
		1000A	1A	20 kW	0.1 kW
		2000A	1A	50 kW	0.1 kW
				100 kW	1 kW
				200 kW	1 kW
				500 kW	1 kW
				1 kkW	1 kW
				2 kkW	1 kW

General Specifications

Size:	9.2 x 3.9 x 2.5 inches (234 x 100 x 64 mm)
Weight:	2.0 lbs (1 kg)
Input Connectors:	
Voltage:	2 shrouded banana jacks (4 mm)
Current Probe:	1 shrouded BNC jack
Battery:	
Type:	4 Alkaline "C" Cells ANSI/NEDA-14A, IEC-LR14 (supplied)
Operating Time:	48 Hours typical (continuous without backlight)

Alternate Battery:

4 NiCad Cells, customer supplied and externally charged. The Tester prevents battery reversal by turning itself off if battery voltage drops below 4.0V dc.

Temperature:		
Operating:	0 to 50°C (32 to 122°F)	
Storage:	-20 to 60°C (-4 to 140°F)	
Temperature Coefficient:	0.1 x Specified Accuracy per °C (0 to 18°C, 28 to 50°C)	
Humidity (noncondensing):		
Operating:	0 - 30°C:	90%
	30 - 40°C:	75%
	40 - 50°C:	45%
Storage:		90%
Altitude:		
Operating:	10,000 feet (2 km)	
Storage:	40,000 feet (12 km)	
Shock & Vibration:	per MIL-T-28800, class 3, sinusoidal, non-operating	
Electro-Magnetic Compatibilty:		
RF Emissions:	EN 50081-1 Commercial Limits, VFG 243-1991	
RF Susceptibility:	EN 50082-1 Commercial Limits	
Council Directive:	Electromagnetic Compatibility Directive (89/336/EEC)	

Drip Proof and Dust Proof Case: per IEC 529, Section 3; IP 52 Dust-Protected, Drip Proof

Display

Type:	Super Twisted Liquid Crystal
Size:	3.0 inch diagonal (76 mm)
Resolution:	160 W x 128 H pixels
Contrast:	User adjustable
Backlight:	Yellow-green LED

Safety

Designed for 600V measurements on industrial power distribution circuits.

⚠ Overload Protection:

Voltage or Current Probe Input:	600V, maximum
Surge Protection:	6 kV per IEC 1010-1
Maximum Voltage Isolation to Earth:	600V from any terminal

Protection Levels:

IEC 1010-1, Pollution Degree 2, Installation Category III, Material Group II, 600V

Protection Class:

Protection Class II as described in IEC 1010-1, Annex H (Double or Reinforced Insulation).

Waveform Memory (Model 41B only)

Eight nonvolatile memories store a maximum of 2048 sampled points of waveform data for both voltage and current inputs for later recall or sending to a computer.

EIA-232-E (RS-232) Interface (Model 41B only)

Optically-Isolated, 1.2, 9.6, or 19.2 baud rate.

Printer graphical output in either Epson or HP format. Text data is sent in ASCII format (SEND). Waveform, Data, and Picture formats may be remotely accessed. Remote Trigger function.

Chapter 2
Theory of Operation

	Title	Page

2-1. Introduction

Chapter 2 provides circuit descriptions for the Fluke 39 Power Meter and Fluke 41B Power Harmonics Analyzer. First, the Tester is described in general terms with a Functional Block Description. Then each block is detailed further with Detailed Circuit descriptions. Schematic diagrams are provided in Chapter 7.

A signal name followed by an asterisk (*) is active (asserted) low. A signal name not followed by an asterisk is active high.

2-2. Functional Block Description

The Tester is unlike most Fluke handheld meters. All waveforms and readings are based on hundreds of measurements instead of a few integrate cycles used in most DMMs. The 128 points used to display waveforms are not directly sampled, but are synthesized using several hundred measurements. This approach allows the instrument to be more flexible and display a wider range of data; such as time and frequency domain data. Using sampled data for watts and RMS values, instead of traditional analog measurement techniques, reduces cost, size, and power consumption. The entire digital section operates on 3.3 volts, which saves power and generates less Radio Frequency Interference (RFI).

Refer to Figure 2-1 during the following functional block descriptions

Tester has seven basic sections:

- Power Supplies
- Input Conditioning
- Analog to Digital (a/d) Conversion
- Digital Kernel (Computer)
- Keypad
- Display
- Optical Interface (Fluke 41B only)

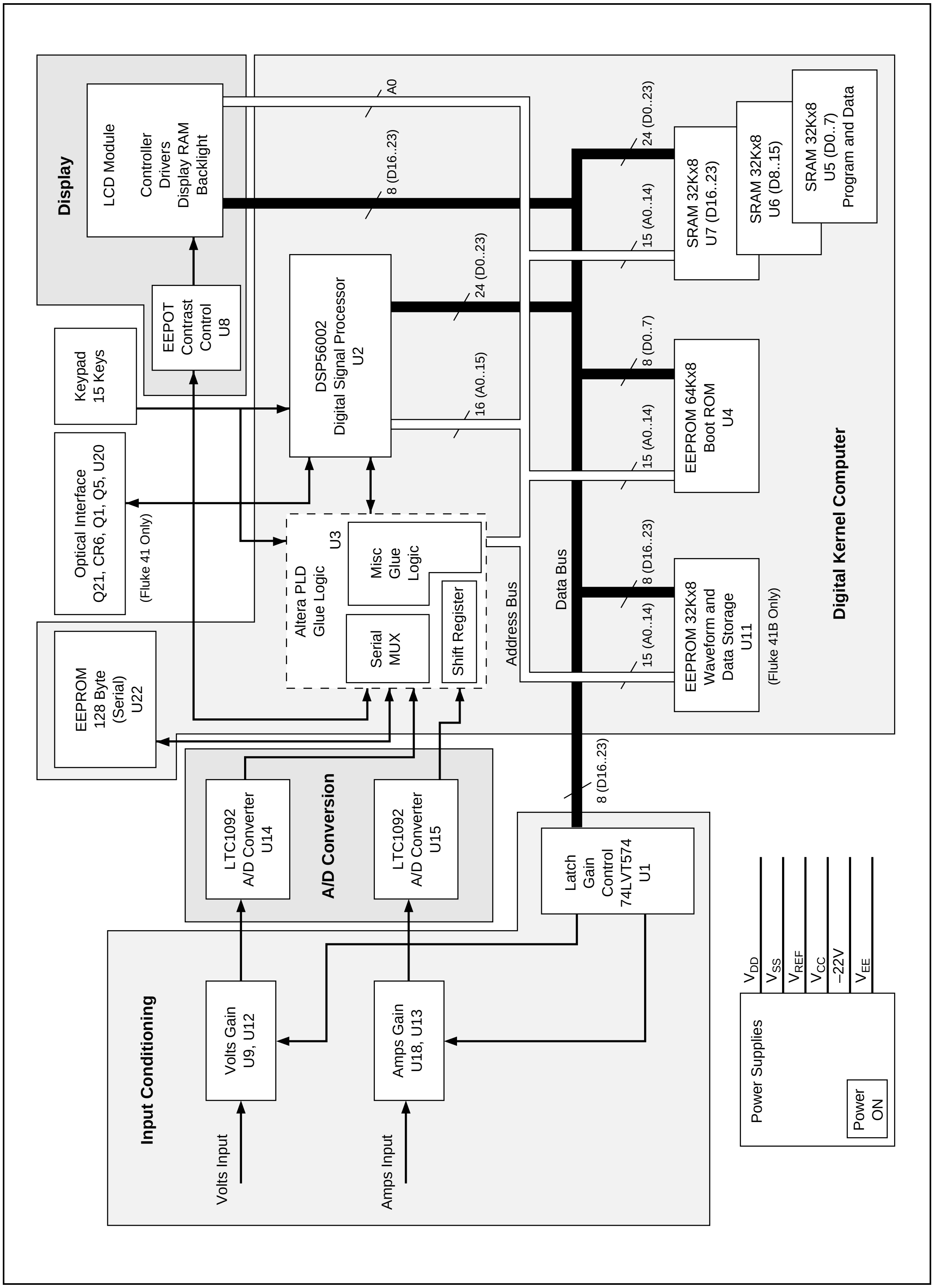

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Figure 2-1. Overall Functional Block Diagram

The power supply voltages for the Tester are derived from four “C” cell batteries. The 4 to 6 volt dc source generates 6 separate voltage sources to power digital, analog, and display circuitry. The “C” cell batteries typically provide 48 hours of Tester operation.

The Input Conditioning section filters and controls the amplitude of the incoming signals to the a/d converters. Signal amplitude is adjusted for maximum dynamic range of the a/d converters. The anti-aliasing filter eliminates any signal components that are more than one half the sampling frequency. Without this filter, some signals may be interpreted incorrectly.

There are two a/d converters in the Tester. One for the volts input and the other for the amps input. These a/d converters quantize the input signals to digital or numeric values, so the Digital Signal Processor (DSP) in the digital kernel can read and process the information. Both converters sample the input signals at a 10 kHz rate.

The digital kernel is basically a small but fast computer system. It has three input sources: sample data from the a/d converters, user input via the keypad, and user input through the serial optical interface. The display is the primary output device, but the digital kernel also controls the input conditioning and sends data to a PC or printer through the optical interface.

The DSP takes the a/d converter samples and stores them in static RAM (SRAM). When enough data samples have been taken, the DSP calculates the values and waveforms for display. No matter what screen is presently on the display, the calculations for all display readings are always performed. The display routines determine which screen the user has selected and displays the appropriate data for the screen requested. All values and waveforms are the result of thousands of calculations performed by the DSP.

The optical interface communicates with a PC or printer, and it provides a sufficient voltage standoff for safety reasons. The Fluke PM9080 interface cable is required to complete the interface to a PC or printer.

2-3. Circuit Operation

To help you understand the circuit operation, the power-up and normal operation sequences are explained below.

2-4. Power-Up Sequence

1. The power button is pressed.
2. The power supply settles to 3.3 volts about 11 ms after the On button is pressed.
3. The reset line (U2-123) changes from high to low about 30 ms after the On button is pressed.
4. The DSP automatically downloads 512 words (1,536 bytes) of instrument operating code to instrument RAM from the EPROM (U4) immediately after coming out of reset.
5. The DSP activates the power-on signal (U2-19) to a high state about 20 ms after coming out of reset.
6. The remaining instrument operating code (about 14K words or 42K bytes) is downloaded from the EPROM (U4) to the SRAM (U5,6,7). This should take about 70 ms or be complete about 100 ms after initial power-up.
7. While the code is being downloaded, a checksum is being calculated. If the check-sum is correct, U2-17 goes high. If there is a problem downloading the program, the unit powers itself off at this point.

8. About 140 ms after the power button is first pressed, a dark screen is displayed. If the power button is held down during power-up, a checkerboard test pattern then appears on the LCD. When the button is released, the instrument resumes normal operation.

2-5. Normal Operation

The normal sequence is as follows:

1. The Tester simultaneously samples volts and amps inputs and stores the samples in SRAM.
2. U2 calculates the results using algorithms stored in the program section of SRAM. The results are stored in SRAM as well.
3. The calculated results are displayed on the LCD. The software determines which mode the instrument is in, and displays the corresponding screen and information.

This entire sequence takes about 300 ms, that is, it repeats about three times per second.

During normal operation, the instrument always operates in this sequence with one exception. When the instrument is in the “HOLD” mode, sampling and calculations are halted until the hold mode is exited, or the display is changed to another screen.

2-6. Circuit Descriptions

2-7. Power Supplies

There are six power sources required for the Tester’s analog, digital and LCD circuits. A +5V dc and -6V dc source is required for the analog section as well as a 2.1154V dc reference voltage for the a/d converters. The digital section requires 3.3V dc for the DSP and associated kernel components. The LCD module requires -22V dc for power and a variable source of -15 to -19V dc to control the LCD contrast. A power-on circuit is incorporated to control the application of power to the various sections of the unit.

2-8. Power-On Circuit

The Tester has a soft key power-on circuit. Closing the power switch turns on Q11. This turns on Q10, which starts the switching regulator (U30). To maintain power to the rest of the circuitry, the microcontroller (U2) sets the signal PWR_ON to a high level (2.4V dc) and starts toggling W_DOG*. When W_DOG* goes low, it turns on Q20, charging C71 to VCC. Q9 remains on as long as the voltage on C71 remains above the threshold voltage (2.15V typical). With Q9 and Q13 both on, Q10 remains on when the power switch is released.

If something causes U2 not to toggle W_DOG*, Q9 turns off after one to three seconds, causing Q10 to turn off and remove power from the instrument. This circuit arrangement allows the instrument to always recover from any microcontroller crash. Q8 signals the microcontroller that the power switch has been pressed after power has been applied. The microcontroller considers this a signal to turn off the instrument.

2-9. VCC

U30 is a buck switching regulator that changes the battery voltage (4V to 6V dc) to the 3.3V dc needed for the digital circuitry. The battery is always connected to the power pin of U30. U30 is in the standby mode until pin 1 goes to the battery voltage level. R31 and C50 set the soft start time. Feedback from the voltage divider (R48 and R41) sets the output to 3.3V dc ±5%. The feedback voltage is ≈1.224V dc. Transformer T1 and capacitor C63 filter the output of U30. U30 has an internal Undervoltage Lockout circuit. The circuit monitors the supply voltage and allows normal operation for voltages greater than 3.75V dc (typical) with 0.25V dc of hysteresis. When an undervoltage is detected, control logic turns off the internal power FET and momentarily grounds C50. This starts a soft start cycle. Circuit operation will not start until the supply voltage (VBT+) goes above 3.95V dc.

2-10. -22 Volts

The raw voltage needed to run the LCD bias is provided by the TLC555 timer (U19), and transformer T2. These two components work as a boost circuit to change the battery voltage to ≈24V dc. Q4, in addition to working in the boost circuit, inverts the 24V dc through CR8, C52, and C68. VR1 controls this voltage to ≈-22V dc. This is necessary because there is no feedback to U19. A feed forward path, R61, helps control the supply voltage as the battery voltage changes. The duty cycle changes, which causes the frequency of the boost circuit to change from 88 to 140 kHz as the battery voltage changes from 4V to 6V dc. The LCD supply is controlled by the microcontroller through signal LCD_PWR, which when high, turns U19 on.

2-11. VEE

The VEE supply controls the contrast of the LCD. U8 is an EEPOT that is controlled by the microcontroller. The voltage appearing at the wiper pin is buffered by an op amp (part of U25). The other half of U25 is used as a difference amplifier to sum the wiper signal with a voltage, which is temperature sensitive. The temperature-sensitive voltage comes from Q18, which is biased as a diode and has a temperature sensitivity of ≈2.2 mV/degree. The default for contrast is ≈-16.6V dc, with a range of -15V dc (minimum contrast) to -18.5V dc (Maximum contrast).

2-12. VDD

The +5V dc supply is generated by first doubling the VCC supply. U29, CR4, C69, and C67 form the voltage doubler circuit. Capacitor C69 is charged to VCC minus one diode drop, when the CAP+ terminal of U29 goes to ground. When the CAP+ terminal goes to VCC, the sum of the voltage across C69 and VCC is applied to C67 through the second diode in CR4. U31 is a low dropout 5V regulator.

2-13. VSS

The negative analog supply (VSS) is generated by U23 and Q12. U23 works by charging C65 to ≈ 6.6V dc, from pin 8 of U23, and then inverts C65 and places it in parallel with C64. Q12 assures that VDD is up before VSS is applied to the analog circuitry.

2-14. VREF

The reference voltage for the two a/d converters is generated by U28, Z5 and U24. U28 provides 2.5V dc ±0.4%. which is divided into 2.1154V dc by Z4. U24 buffers the reference voltage (2.1154V dc) for use by the a/d converters and their input dividers.

2-15. Low Battery Detection

The low battery detection circuit monitors the battery voltage and sends a signal to the microcontroller when the battery voltage falls below 4.22 volts. R49 and R53 set the reference for the circuit to 1.47 volts. R52 and R30 divide the battery voltage down to stay within the common mode range of the op amp. R58 provides hysteresis, to prevent oscillations. LOW_BAT goes low when the battery drops below its minimum value.

2-16. Power Reset

Various parts of the digital circuitry require a power reset signal to initialize their operation upon power-up. U26 and Q19 monitor the VCC power supply. When the VCC voltage goes above ≈2.7 Volts, Q19 turns on. This causes Q17 to turn off and allows C46 to start charging. When the voltage across C46 reaches ≈1.8V dc, Q2 turns on, pulling the RESET signal low. Because both senses of the reset signal are needed, Q3 inverts the RESET signal and provides the signal RESET*.

2-17. Input Conditioning

Both the voltage and current inputs provide gain adjustments and filtering of the incoming signal before it is sent on to the a/d converters.

2-18. Difference Amplifier (Voltage Input)

U10 and Z6 form a difference amplifier. The difference amplifier improves the instrument's operation on three-phase delta power systems. It also provides isolation and a protective impedance in both the high and common inputs. The gain of the amplifier is 1/500.

2-19. Protection Circuit (Current Channel)

RT1, R38, R18, R23. R17, Q6, and Q7 form a protection circuit to limit the input voltage and current applied to U18 during accidental overvoltages. The emitter of Q7 clamps any input voltage to ≈ ±10 Volts. R17 further limits the current into the input of U18 to 500 µA.

2-20. Gain Amplifier

Both the voltage and current inputs adjust the gain based on the range selected. There are three hardware ranges for each input; 256, 512, and 1024 volts peak for the voltage input, and 20, 200, and 2000 Amps peak for the current input. The ranges for the current input assume that the input is 1 mV/Amp. The gain for both inputs are controlled by the microcontroller through a latch (U1). Resistor networks Z4 & Z7 are ratio matched to 0.1%, with the resistor between pins 1 and 8 as the reference.

2-21. Latch (U1)

The latch (U1) controls the switches that select the gain for both the amps and volts input stages. The switches controlled by U1 change the feedback path of the amplifiers U9 and U18, thus changing the gain. The D inputs to the latch are directly connected to the DSP bus. The signal to latch the data is generated by U3 (CS_GAIN). The latch is memory mapped in the "Y" data space at address $FFD0.

Tables 2-1 and 2-2 show the relationship between the control signals and the selected gain.

Table 2-1. Voltage Gains

Range	Signal	Gain	Software Limit
256V	X4 (low)	Four	200V peak
512V	X2 (low)	Two	500V peak
1024V	X1 (low)	One	937V peak

Table 2-2. Current Gains

Range	Control Signals				Gain	Software Limit
	X1A	X10A	X1B	X10B		
20A peak	1	0	1	0	100	20A peak
200A peak	1	0	0	1	10	200A peak
2000A peak	0	1	0	1	1	2000A peak

2-22. Anti-Alias Filter

There are two anti-aliasing filters: one for volts (U16) and the other for amps (U17). The anti alias filter consists of both sections of U16 or U17 and the resistors and capacitors that are connected to them. The purpose of the filter is to attenuate any input frequencies that are near or above one half of the sample rate of the a/d converters. The filter is a 4-pole Butterworth, consisting of a cascade of two second-order low-pass filters. The filter has unity gain from DC to 2.015 kHz (±0.2 dB). The 3 dB point of the filter is at 3.5 kHz. The filter should have ≈19 dB (± 0.5 dB) of attenuation at 6 kHz.

2-23. Level Shifter

Z8 translates the input signal from a bipolar signal, with full scale range of ±2 volts peak, to an unipolar signal that goes from 0 to 2 volts. The output of the divider should be at one half of VREF when the input is at zero volts. The resistors in Z8 are ratio matched to 0.1%, with the resistor between pins 1 and 8 as the reference.

2-24. A/D Converters

The two a/d converters are 10-bit successive approximation converters. One measures volts and the other measures amps. These parts use serial interfaces to communicate to the DSP through U3's serial Multiplexer section. When CS_AD* goes low, the a/d converter starts a conversion cycle. CS_AD* stays low during each conversion cycle. During the conversion cycle, 12 bits are read by the microcontroller. The a/d converter sends the two Least Significant Bits twice. The data is sent Most Significant Bit first. The a/d converter sample rate is 10.076 kHz and the clock rate is 241.824 kHz. Resistor R71 is needed to limit the current between the a/d converter and the microcontroller because the a/d converter operates at 5 volts, while the microcontroller operates at 3.3 volts.

2-25. Digital Kernel

The digital kernel consists of a digital signal processor, a programmable logic device (PLD), ROM, and RAM. It processes the input signals from the a/d converters, computes the values and waveforms, and stores the data in RAM for the display.

2-26. Digital Signal Processor (U2)

The DSP56002 processor (DSP) has full control of all hardware in the Tester. It controls a/d sampling, computations, serial interface, user interface, and the display.

The DSP has several I/O ports that can be configured in a number of different ways. Two of these ports are for serial communications. The Fluke 41B makes use of one serial port for RS-232 communication to printers or PCs over a special optical interface and cable. The second serial port is used by both models to communicate to the two a/d converters (U14 and U15) and the serial EEPROM (U22). The other I/O ports are used for various control and sensing: keypad interface, power control, low battery sense, and memory bank switching.

This DSP, unlike most common microcontrollers, is optimized for calculations instead of control. The data bus is 24 bits wide. All internal data registers are 24 bits, except two accumulators which are 56 bits wide.

There are three 64K address spaces that share the same external address and data bus. The three address spaces are Program, X-data, and Y-data. Code can only be executed from the program space, but data can be stored and retrieved from all three address spaces. The control lines DS*, PS*, and X/Y* from the DSP, control which of these three address spaces are accessed. Although this may sound a bit complex with the three address spaces, you could think of the PS* and X/Y* signals as two more address lines (A16 and A17)

2-27. Programmable Logic Device

A Programmable Logic Device (PLD) replaces several generic parts that usually consume more board space and power. Much like a ROM, these parts can be programmed into an almost limitless combination of circuits. This makes them easy to use, but sometimes hard to debug, since they look like a black box from the outside. In the case of the Fluke 39/41B, U3 is broken into six relatively simple sections. Several of the sections share common inputs. Figure 2-2 is a block diagram of the internal circuits of the PLD.

2-28. Keypad Interrupts

The four row signals (R0-3) from the keypad are ANDed together. If any of the signals drop below a valid high state, IRQA* is driven low. This generates an interrupt to the DSP so that the software does not have to continually scan the keypad inputs until an interrupt is detected.

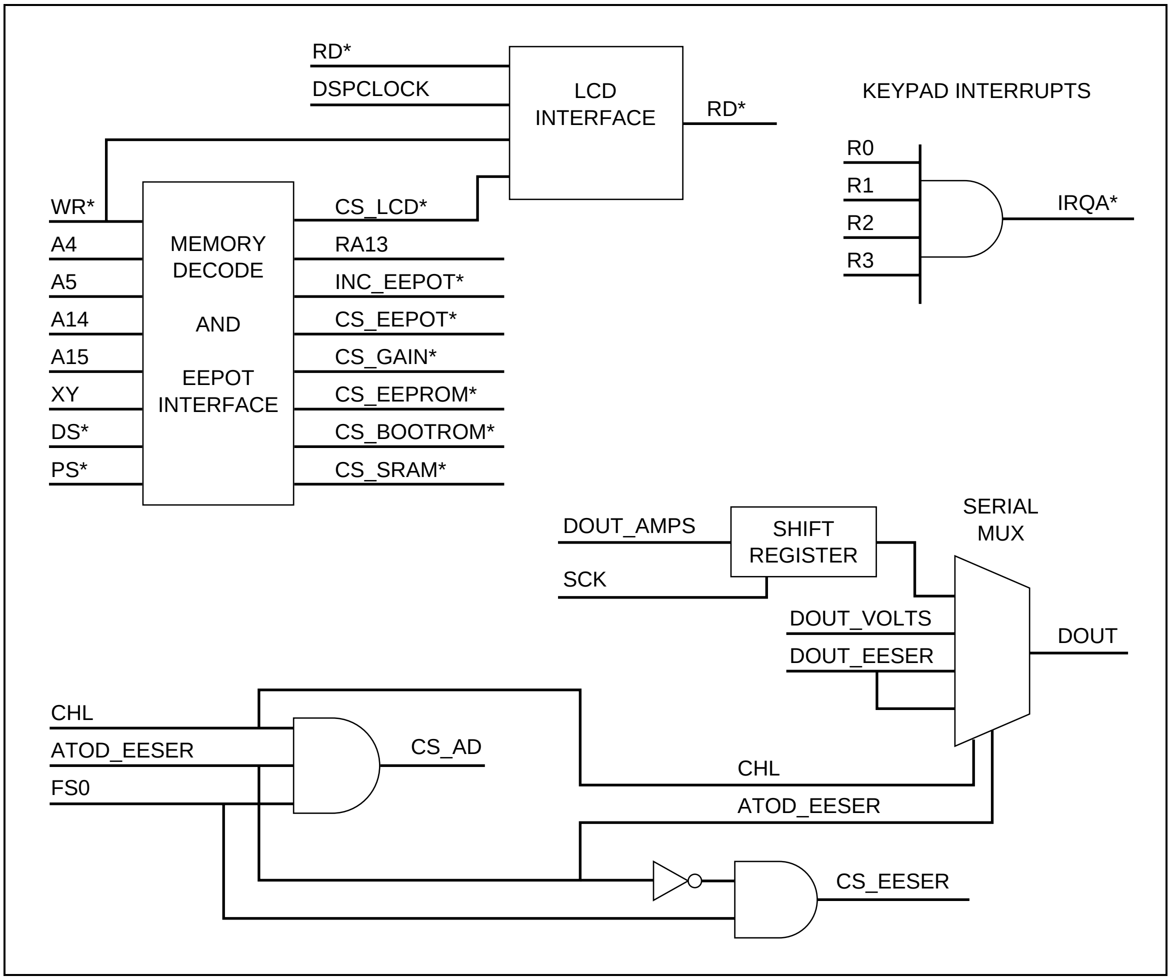

Figure 2-2. PLD Block Diagram

2-29. Memory Decoding

The signals A15, A14, A5, A4, PS*, DS*, XY, and WR* are used to map out the SRAM, EPROM, EEPROM, Gain Latch, EEPOT, and LCD in program and data space. Although the SRAM looks like one contiguous RAM space, it's actually divided into three separate memory spaces. Table 2-3 shows where external memory and I/O are mapped.

Table 2-3. Memory Map

Device	X Data Space	Y Data Space	Program Space
SRAM (U7-5)	$8000 - $9FFF	$8000 - $9FFF	$0000 - $1FFF $4000 - $5FFF
EPROM (U4)			$8000 - $FFFF
EEROM (U3)	$4000 - $7FFF		
LCD		$FFC0 - $FFC1	
LATCH (U1)		$FFD0	
EEPOT (U8)		$FFE0, $FFF0	

Table 2-4 is a truth table for the selection of the various devices in the Tester.

Table 2-4. Logic Truth Table

Device	Signal	A4	A5	A14	A15	DS*	PS*	XY
SRAM	CS_SRAM				0		0	
SRAM	CS_SRAM			0	1	0		
EEPROM	CS_EEPROM			1	0	1		1
EPROM	CS_BOOTROM				1		0	
LCD	CS_LCD	0	1	1	1	0		0
EEPOT	INC_EEPOT	0	1	1	1	0		0
EEPOT	CS_EEPOT	1	1	1	1	0		0
LATCH	CS_GAIN	1	0	1	1	0		0

2-30. Interface to LCD Module

The LCD module requires a clock sync signal “E” that synchronizes all read and write operations. It signals the display module that all address, data, and control signals are valid, with an active high state. This signal is generated from U2 signals WR*, RD*, DSPCLOCK, and CS_LCD*. This generated “E” signal is active high during a read/write operation between the DSP and the LCD module.

2-31. Shift Register

The amps and volts readings are sampled simultaneously to avoid phase errors. The a/d data for both input channels is transferred to the DSP over a single serial port. The PLD shift register stores an amps data point while the DSP is reading the associated volts data point.. After the volts data point has been read into the serial port, the data from the shift register (amps data) is clocked out and read. This process repeats until the until the appropriate number of samples have been read.

2-32. Serial Multiplexer

There are three sources of serial data; the volts a/d converter, the shift register holding the amps data input, and the serial EEPROM (U22). The DSP signals the PLD multiplexer to select one of the three sources and feed that source (DOUT) to the single serial port on the DSP.

2-33. EEPOT (Contrast Control) Interface

The EEPOT interface of the PLD provides the chip select (CS_EEPOT*) and the control (INC_EEPOT*) signals for the EEPOT. The signal that controls the direction of the wiper comes directly from the DSP. Reading or writing to address location Y:$FFE0 enables CS_EEPOT and strobes the INC_POT signal. After the correct value is reached, location Y:$FFF0 is read or written to clear the CS_EEPOT, which writes the value into the EEPOT.

2-34. SRAMs (U5,U6,U7)

The SRAM is used for two main functions: operating code storage and sampled and calculated data storage. After the Fluke 39/41B has completed its initialization and is running, program execution is directly from one program section of the SRAM. Storage of all sampled and calculated data is stored in the X and Y data spaces.

The 96 kilobytes (32 kilowords x 24 bits) of static RAM is divided into three sections: Program, X-data, and Y-data. The Y-data space uses 8K words, X-data space uses 8K words, and Program space uses the remaining 16K words. The first 0.5K word (P:0000..1FF) of Program space is on the DSP chip (U2).

2-35. EPROM (U4)

The EPROM contains the instrument software. During start-up 512 words (1536 bytes) are read from the EPROM and then executed from within the internal DSP program RAM. The remaining portion of the 16K words is downloaded into the program space of the SRAM. After boot-up, the EPROM is not accessed again until the unit is powered up again.

Although U4 is an EPROM, it cannot be reprogrammed, since it is not a windowed part. This type of EPROM is know as an OTP or One Time Programmable.

2-36. EEPROM (U11)

The EEPROM (U11) provides a nonvolatile storage of waveform and calculated data for the Model 41B’s memory feature.

2-37. Serial EEPROM (U22)

The serial EEPROM (U22) provides non-volatile storage of calibration constants, power-up defaults, and display contrast constants.

2-38. Keypad

The keypad consists of 15 individual keys in a 4x4 matrix. When a key is pressed, one of the 16 possible points in the matrix is shorted together. The rows of the matrix are pulled up to Vcc with 30 kΩ resistors in Z2. The columns are normally at a low state, which is controlled by the DSP. The total resistance of the switch as seen at the pca should be less than 3 kΩ. The contact resistance itself is only about 200Ω, but there are several other virtual resistors in the circuit, including the elastomeric connector that contacts the keypad to the pca. The normal voltage at the four row lines is Vcc, when no keys are pressed. When a key is pressed, the corresponding row is pulled down to about 0.4V dc. The four row signals are also connected to U3. If U3 senses that any of the row signals is in a low state, it generates an interrupt to the DSP. By applying a logic low to the columns one by one, the DSP can determine the pressed key.

2-39. Display

The Fluke 39/41B display consists of two circuits, the LCD Module and the Contrast Control.

2-40. LCD Module

The LCD module is a complete system. It contains the liquid crystal, LCD drivers, controller, display RAM, backlight, and hardware to hold it together as a module. The LCD module connects to the rest of the system with a 24 conductor flat cable. Extra logic was required to interface the display control lines to a fast DSP. This logic resides in the PLD (U3).

Specifications:

- x 128 pixels (W x H)
- FSTN (Film-Compensated Super Twisted Nematic)
- LED backlight
- 32K x 8 display RAM
- Integrated 1335 controller

2-41. BackLight

The backlight is a series of 24 yellow-green Light Emitting Diodes (LEDs). The diodes are connected two in series and 12 in parallel. The backlight control circuit switches the current and sets the level of the current to the diodes. Q15, R51, R55, R57, and R60 form a level shifter to turn on control transistor Q16. When Q16 turns on, it establishes a reference voltage of 100 mV at the noninverting input of U21. U21 through Q14 forces 100 mV across the parallel combination of R54 and R59. This action causes the current through the back light to be ≈40 mA.

2-42. Contrast Control - EEPOT (U8)

The Contrast Control EEPOT is functionally the same as a regular potentiometer, except that the wiper location is controlled via a digital interface instead of a knob. The digital interface to this part consists of three lines, chip select (CS), increment wiper (INC*), and up/down (U/D*). To adjust the potentiometer, CS is brought low and the INC line is strobed. The direction of the wiper is dependent on the state of the U/D* pin. U8 is configured as a simple voltage divider and controls the voltage supplied to the LCD module. This voltage varies from about -13V dc to -20V dc. The EEPOT setting is also stored to serial EEPROM (U22). If an invalid EEPOT value is read from the serial EEPROM, a default value is used. If a too light value is read, a minimum contrast value is used.

2-43. Optical Interface (Model 41B Only)

This interface consists of two main sections: the receiver and the transmitter. Data going out of the unit is transmitted through a infrared LED. Incoming data is captured through a photo transistor in the receiver.

2-44. Transmitter

CR6 is an infrared emitter used to communicate with an optical RS-232 interface cable provided with the Fluke 41B. The transmitter circuit is a simple level shifter used to provide more current to the LED, than the DSP can provide directly. Q21 is used as a current switch to turn CR6 on and off. When TXD on the microcontroller goes low, Q21 turns on, and the current through CR6 is set by the resistor R36 and the voltage across CR6. The current through CR6 should be ≈11 mA at ambient.

2-45. Receiver

Q5 is a photo transistor used to receive the signal provided by the Fluke 41B’s RS-232 cable. It senses the infrared light from the infrared LED in the optional interface cable. When an infrared light source is on, Q5 begins to conduct harder, which turns on Q1. Q1 provides the necessary current gain to interface the received signal with the microcontroller. U20 provides a variable collector supply voltage to Q5. R25 and C10 filter the signal at the collector of Q1. The DC value of the signal is compared with the diode voltage of CR1. U20 integrates the error voltage and sets the voltage at the collector of Q5. C11 is an additional filter for the collector voltage of Q5. The voltage at the collector of Q5 is ≈2V dc with no light and should go to 0V dc if light is shown continuously on Q5.

Chapter 3
General Maintenance

Warning

Service procedures in this chapter should be performed by qualified personnel only. To avoid electrical shock, do not service this product unless you are qualified to do so.

3-1. Introduction

This chapter provides handling, cleaning, disassembly, and assembly instructions.

3-2. Warranty Repairs and Shipping Information

If your Tester is still under warranty, see the warranty information at the front of this manual for instructions on returning the unit. The list of authorized service facilities is included in Chapter 6.

3-3. General Maintenance Information

3-4. Required Equipment

Equipment required for calibrating, troubleshooting, and repairing the Tester is listed in Chapter 4 (Table 4-1).

3-5. Static-Safe Handling

All integrated circuits, including surface mounted ICs, are susceptible to damage from electrostatic discharge (ESD). Modern integrated circuit assemblies are more susceptible to damage from ESD than ever before. Integrated circuits today can be built with circuit lines less than one micron thick, allowing more than a million transistors on a 1/4-inch square chip. These submicron structures are sensitive to static voltages under 100V. This much voltage can be generated on a dry day by simply moving your arm. A person can develop a charge of 2,000V by walking across a vinyl tile floor, and polyester clothing can easily generate 5,000 to 15,000V during movement against the wearer. These low voltage static problems are often undetected because a static charge must be in the 30,000 to 40,000V range before a person will feel a shock.

Most electronic components manufactured today can be degraded or destroyed by ESD. While protection networks are used in CMOS devices, they can only reduce, not eliminate, component susceptibility to ESD.

ESD may not cause an immediate failure in a component; a delayed failure or "wounding" effect is caused when the semiconductor’s insulation layers or junctions are punctured. The static problem is, therefore, complicated in that failure may occur anywhere from two hours to six months after the initial damage.

Two failure modes are associated with ESD. First, a person who has acquired a static charge can touch a component or assembly and cause a transient discharge to pass through the device. The resulting current ruptures the junctions of a semiconductor. The second failure mode does not require contact with another object. Simply exposing a device to the electric field surrounding a charged object can destroy or degrade a component. MOS devices can fail when exposed to static fields as low as 30V.

Follow these two rules for handling static-sensitive devices:

1. Handle all static-sensitive components at a static-safe work area.

   Use grounded static-control table mats on all repair benches, and always wear a grounded wrist strap. Handle boards by their nonconductive edges only. Store plastic, vinyl, and Styrofoam objects outside the work area.

2. Store and transport all static-sensitive components and assemblies in static-shielding bags or containers.

   Static-shielding bags and containers protect components and assemblies from direct static discharge and external static fields. Store components in their original packages until they are ready for use.

3-6. Cleaning

Warning

To avoid electrical shock or damage to the tester, never allow water inside the case. To avoid damaging the tester's housing, never apply solvents to the meter.

When the Tester requires cleaning, wipe it with a cloth that is lightly dampened with water or a mild detergent. Do not use aromatic hydrocarbons, chlorinated solvents, or methanol-based fluids when wiping the Tester.

3-7. Disassembling the Tester

The following paragraphs describe how to disassemble the Tester to the pca level. Start and end your disassembly at the appropriate heading levels.

Caution

Always remove the case bottom first to avoid damaging the Tester.

3-8. Removing the Meter Case Bottom

Perform the following procedure to remove the case bottom (Figure 3-1).

1. Make sure the Tester is disconnected from any live source, turned off, and all test leads are removed from the input module.
2. Remove the two slotted screws on the battery cover (one is located under the hook) and remove the cover.
3. Remove the batteries.
4. Remove the six Phillips screws from the case bottom.
5. Insert a thin non-sharp object (e.g., credit card or plastic tuning tool) between the case bottom and the input module, and gently pry the case bottom away from the input module. (Figure 3-1) When the seal between the case bottom and the input module breaks, the case bottom will free itself.

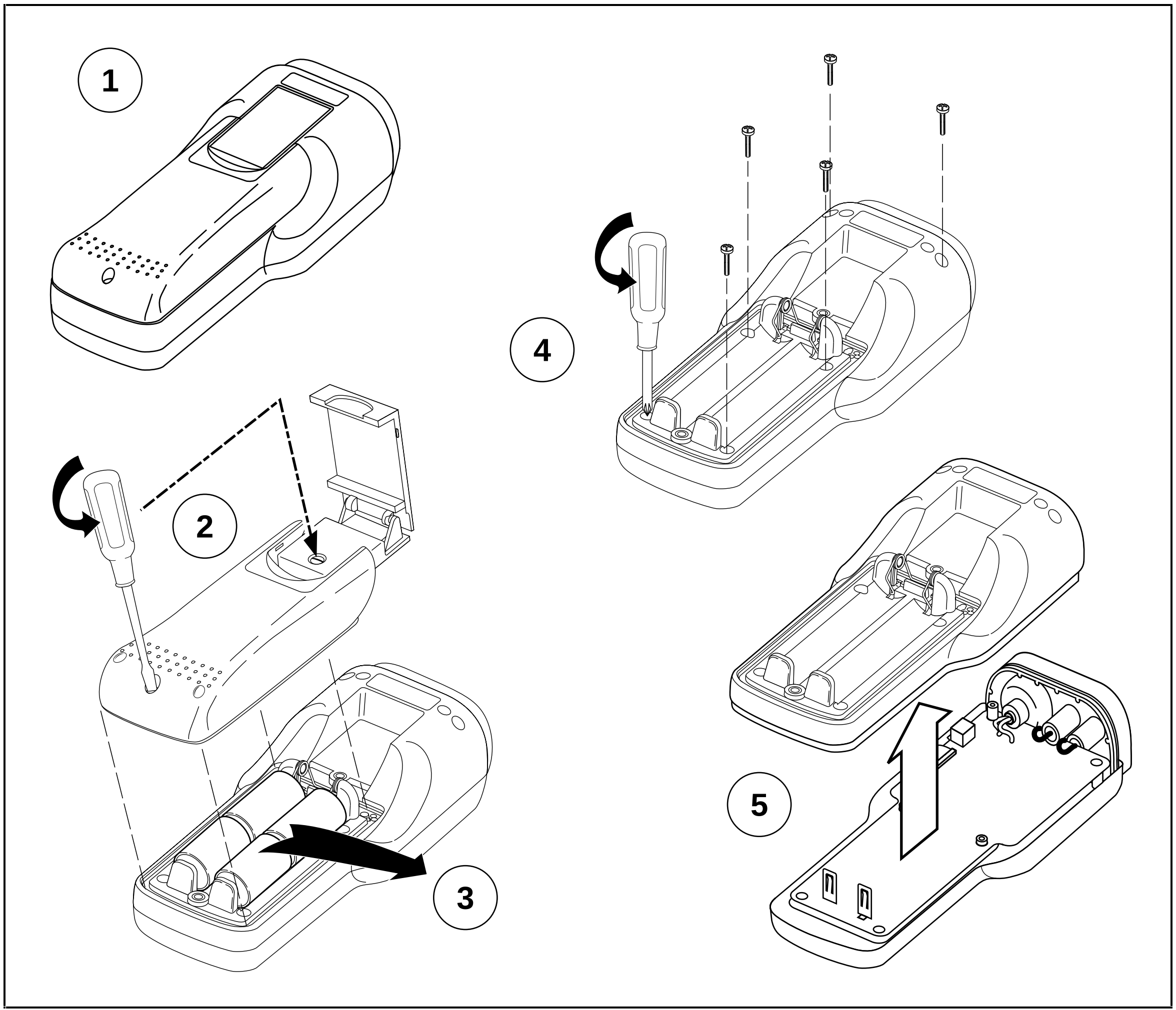

Figure 3-1. Removing the Case Bottom

3-9. Removing the PCA and Input Module

Caution

To avoid contaminating the pca with oil from your fingers, handle the pca by its edges or wear gloves. A contaminated pca may not cause immediate instrument failure in controlled environments. Failures typically show up when contaminated units are operated in humid areas.

After you have removed the case bottom, use the following procedure to remove the pca and input module:

1. Before removing the board from the case top, disconnect the flex cable from the board by pulling out the connector latch from the connector body. (Figure 3-2). The latch remains attached to the connector body.
2. Pull the input module away from the case top. The input module remains attached to the pca.
3. Lift the pca and input module out of the case top. The flex cable pulls away from the connector when the pca is lifted out of the case.

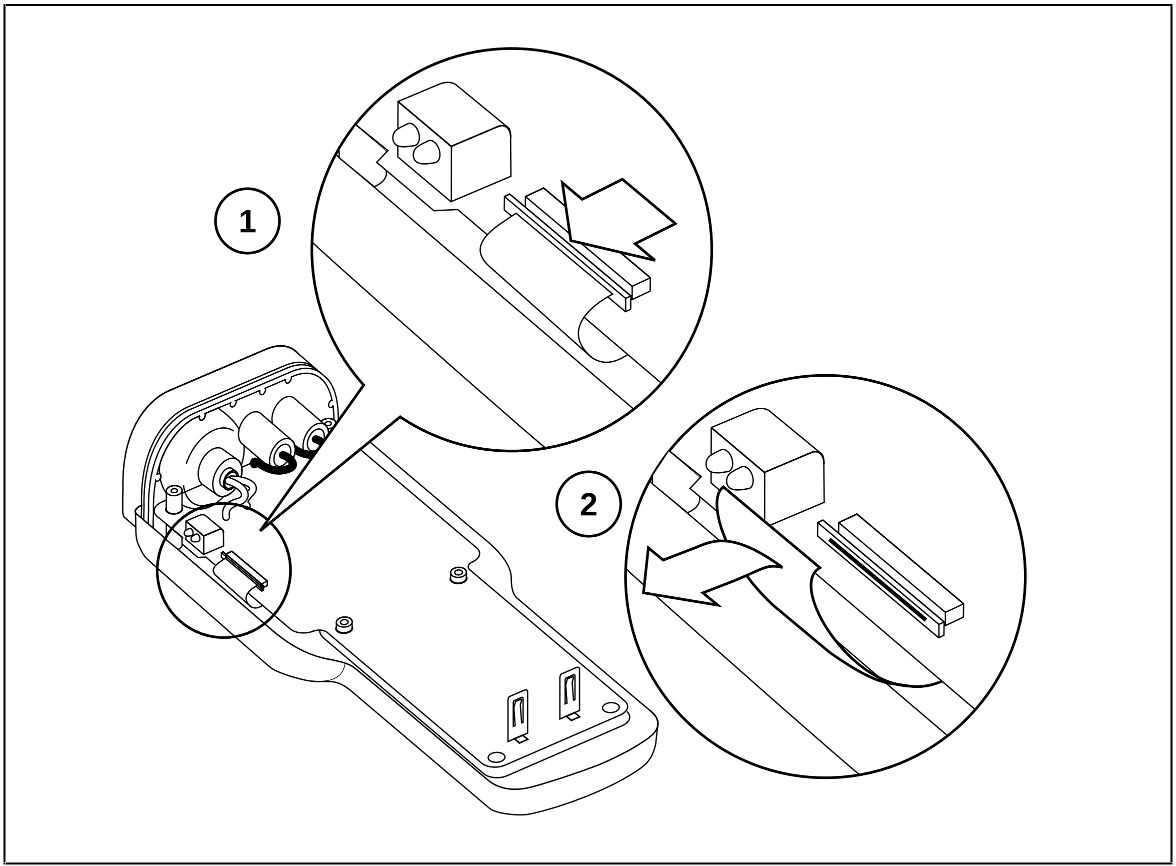

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Figure 3-2. Flex Cable Connector

3-10. Removing the LCD Module

After you have removed the case bottom and pca, use the following procedure to remove the LCD module:

1. Remove the four Phillips screws from the corners of the LCD module.
2. Lift the LCD module out of the case top.

3-11. Removing the Elastomeric Keypad

After you have removed the case bottom and pca, lift the Elastomeric keypad out of the case top.

3-12. Reassembling the Tester

Generally, reassembling the Tester is the reverse of disassembly. However, you must follow special precautions when installing the pca and input module.

3-13. Installing the PCA and Input Module

1. With the pca held outside the case top and the flex cable connector latch pulled out, insert the free end of the flex cable into the connector. Make sure that the flex cable is fully engaged. Push the connector latch back against the connector body.

2. Rotate the pca into the case top, aligning the holes in the pca over the six bosses. Make sure that the pca is pressed down over the ribs of the boss in the upper right corner of the case top.
3. Align the top edge of the input module with the sealing groove on the case top. While ensuring the input module remains squarely within the side walls of the case top, press the input module into the groove until it seats snugly against the top edge of the case top.
4. Ensure the four leads from the input module remain connected to the pca. The black wire must be dressed so that it wraps counterclockwise into the connector. Both the black and red wire must be dressed so they bend outward toward the side of the case and are not between the pca and the plastic cylinders of the input module.

3-14. Reassembling the Case Bottom

1. Align the bottom edge of the input module with the sealing groove on the case bottom. While ensuring the input module remains squarely within the side walls of the case bottom, press the case bottom onto the input module until it seats snugly against the top edge of the case bottom.

   If the case bottom gets cocked at an angle to the sides of the input module, the case top and case bottom will not come together properly. Make sure the case bottom and case top are firmly pressed together. The gap width on either side of the instrument, between the case bottom and case top, should be approximately equal.
2. Reinstall the six Phillips screws into the case bottom.
3. Reinstall the batteries and fasten the battery cover in place using the two slotted screws.

Chapter 4
Performance Testing and Calibration

Title		Page

Warning

Service procedures in this chapter should be performed by qualified service personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.

4-1. Introduction

This chapter provides calibration and performance tests that allow you to verify that the Tester is operating within published specifications.

4-2. Required Equipment

The equipment in Table 4-1 is required for performance testing and calibration. If the recommended models are not available, equipment with equivalent specifications should be used.

Table 4-1. Recommended Test Equipment

Equipment Type	Minimum Specifications	Recommended Model
Calibrator A, volts	**DC Voltage:** Range: 1 mV - 600V Accuracy: 0.12% **AC Voltage:** Range:1 mV - 600V Frequency: 60 Hz Accuracy: 0.12%	Fluke 5700A Fluke 5500A
Calibrator B, volts*	**AC Voltage:** Range: 30 mV-1.4V Frequency: 60 Hz Accuracy: 0.12%	Fluke 5200A Fluke 5500A
Phase meter*	Phase accuracy: 0.5 degrees @ 60 Hz comparing 10 mV and 5 V inputs	Clarke-Hess Model 6000A Fluke 5500A
Dual channel signal generator*	**AC Voltage:** Range: 50 mV - 20 V p-p Frequency: 60 Hz Accuracy: 0.5% Phase accuracy: 0.5 degrees @ 60 Hz sourcing 10 mV and 5 V inputs	Fluke 5500A
* A second calibrator, phase meter and dual channel signal generator is not required when using one Fluke 5500A Multi-Product Calibrator.		

4-3. Performance Tests

If the Tester passes the following tests, the meter is in proper operating condition. If the meter fails any of the performance tests, calibration adjustment and/or repair is needed.

4-4. Warming-Up the Tester

Before performing any of the following performance tests, the Tester should be allowed to sit for four hours in an environment of 18-28° C with a relative humidity of less than 70%. Once adjusted to the environment, turn on the Tester and allow it to warmup for at least 2 minutes.

4-5. Checking the Display Pixels

To check the Tester's diplay pixels, press and hold ⓘ. The Tester displays a uniform checkerboard pixel pattern. Visually check the pixel pattern for missing pixels. When done, release ⓘ and the Tester will start normal operation. If the display is not at a viewable level, change the contrast setting to a normal level and repeat.

Note

The following procedures are based on using two calibrators, a phase meter and a dual channel signal generator. Other test equipment configurations may require some adjustments in the performance tests and calibration procedures described in this chapter.

4-6. Testing Voltage Performance

Perform the following procedure to test the voltage function of the Tester.

Warning

Ensure that the calibrator is in standby mode before making any connection between the calibrator and Tester. dangerous voltages may be preSent on the leads and connectors.

1. Connect a cable from the Output Voltage HI and LO connectors of calibrator "A" to the V and COM connectors on the Tester.
2. Press [TEXT] until the text screen is displayed.
3. Press [V A W] until V is diplayed in the upper right corner of the display.
4. Press [V Ø A REF] until VØ is displayed in the top status line of the Tester.
5. Set the output of calibrator "A" to the Calibrator Output values in Table 4-2. DC voltages are listed in the upper section of the table and AC voltages at 50 or 60 Hz, whichever is your local line frequency, are listed in the lower section of the table. Blank fields do not need to be evaluated.

Note

Apply the voltage incrementally so the Tester does not autorange to the next higher range. Ensure the Tester is in the appropriate range before checking the reading against the performance limits.

6. Verify that the readings are within the minimum and maximum limits specified in Table 4-2.

Table 4-2. Volts Performance

Calibrator Output	**Fluke 39/41B Range**	**Performance Limits**					
		V rms		**V pk**		**V dc**	
V dc		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
5.00V	20					4.4	5.6
15.0V	50					14.4	15.6
65.0V	100					63.4	66.6
130.0V	200					127.1	132.9
208.0V	500					201	215
350.0V	500					340	360
480.0V	1000					467	493
600.0V	1000					585	615
V ac							
5.00V	20	4.5	5.5	6.5	7.7		
15.0V	50	14.7	15.3	20.5	22.0		
65.0V	100	64.4	65.6	89.8	94.1		
130.0V	200	129.1	130.9	179.9	187.8		
208.0V	500	205	211	285	303		
350.0V	500	346	354	483	507		
480.0V	1000	475	485	662	695		
600.0V	1000	595	605	828	868		

4-7. Testing Amps Performance

Perform the following procedure to test the amps funtion of the Tester.

Warning

Ensure that the calibrator is in standby mode before making any connection between the calibrator and Tester. dangerous voltages may be preSent on the leads and connectors.

1. Press [HOLD ENTER] and turn on the Tester to enter the Setup screen.
2. Using [HOLD ENTER] and [◁] [▷] , select “OTHER” for Clamp Setting.
3. Press [HOLD ENTER] to exit the Setup screen.
4. Connect a cable from the Output Voltage HI and LO connectors of calibrator “A” to the Current Probe connector on the Tester.
5. Press [TEXT] until the text screen is displayed on the Tester.
6. Press [V A W] until A is displayed in the upper right corner of the display.

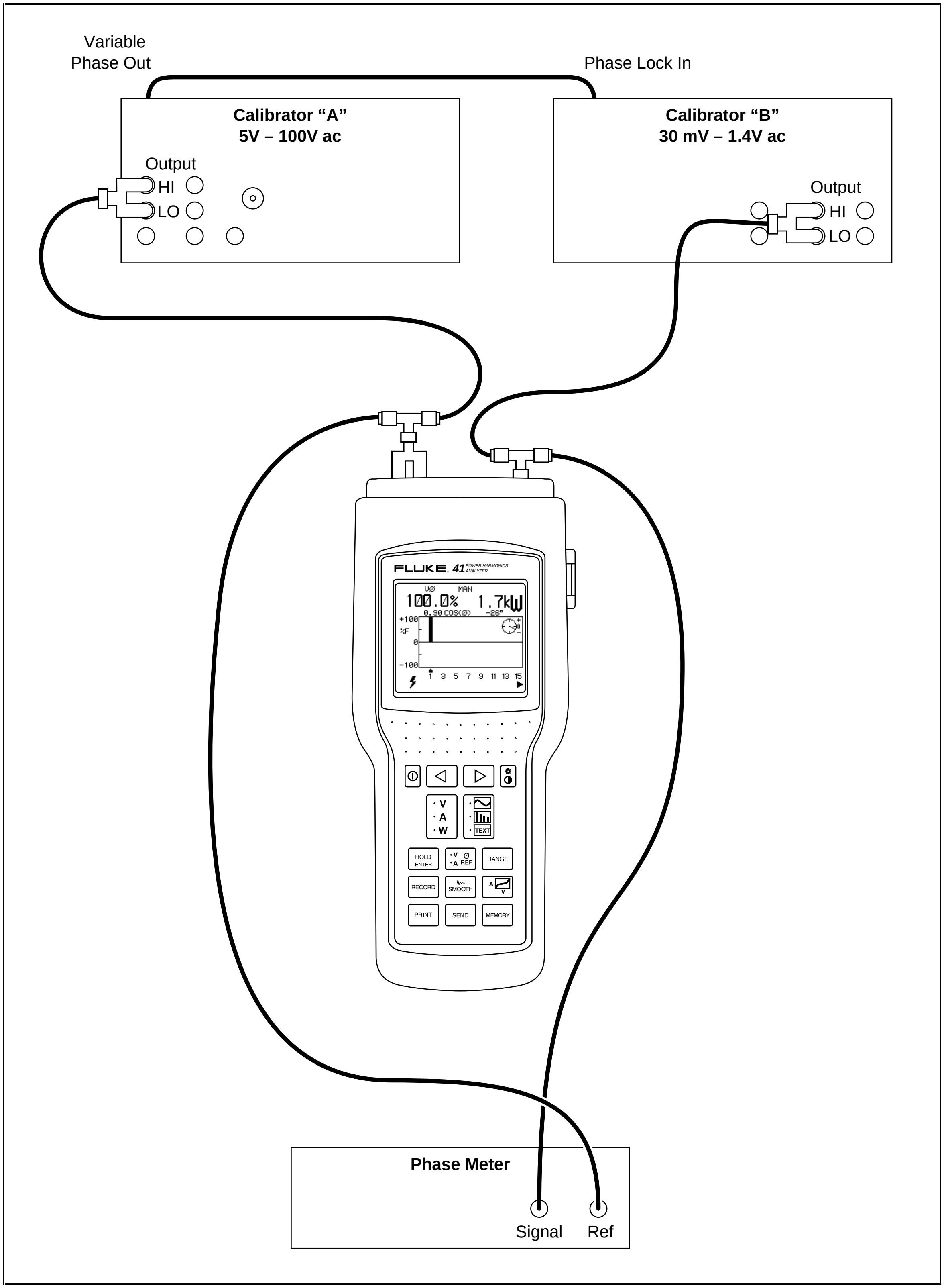

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Figure 4-1. Watts Performance Test Configuration

7. Press [V A REF] until A.Ø is displayed in the top status line of the Tester.
8. Set the output of calibrator "A" to the Calibrator Output values in Table 4-3. DC voltages are listed in the upper section of the table and AC voltages at 50 or 60 Hz, whichever is your local line frequency, are listed in the lower section of the table. Blank fields do not need to be evaluated.

Note

Apply the voltage incrementally, so the Tester does not autorange to the next higher range. Ensure the Tester is in the appropriate range before checking the reading against the performance limits.

9. Verify the readings are within the minimum and maximum limits specified in Table 4-3.

Note

*It is normal for the tester to display "**OL*%THD*" with a VDC input.*

Table 4-3. Amps Performance

Calibrator Output	Fluke 39/41B	Performance Limits					
		A rms		A pk		A dc	
mV dc	**Range**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
1.00 mV	2					0.94	1.06
6.70 mV	10					6.52	6.88
13.50 mV	20					13.19	13.81
67.00 mV	100					65.2	68.8
135.0 mV	200					131.9	138.1
670.0 mV	1000					652	688
1000.0 mV	2000					976	1024
mV ac							
1.00 mV	2	0.96	1.04	1.34	1.49		
6.70 mV	10	6.63	6.77	9.25	9.71		
13.5 mV	20	13.40	13.60	18.67	19.52		
67.00 mV	100	66.3	67.7	92.5	97.1		
135.00 mV	200	134.0	136.0	186.7	195.2		
670.0 mV	1000	663	677	925	971		
1000.0 mV	2000	992	1008	1381	1447		

4-8. Testing Watts, VA, VAR Performance

Perform the following procedure to test the watts, VA, and VAR functions of the Tester.

Warning

Ensure that the calibrator is in standby mode before making any connection between the calibrator and Tester. dangerous voltages may be preSent on the leads and connectors.

1. Connect the equipment as shown in Figure 4-1. Calibrator “A” should have a range of 5V to 100V ac and calibrator “B” should have a range of 35 mV to 1.4V ac.
2. Set the output amplitude from the calibrators, to the values in Table 4-4.
3. Enable the Phase Lock mode on calibrator “B”.
4. Using the Phase Shift function on calibrator “A”, adjust the phase to within ±0.5 degrees of the phase shift specified in Table 4-4.
5. Press V/A/W until W is displayed in the upper right had corner.
6. Press TEXT until the Tester is in the Text Screen mode. Verify that the W/KW, VA/KVA and VAR/KVAR readings are within the minimum and maximum limits specified in Table 4-4.
7. Press TEXT until the Tester is in the Harmonics screen mode. Verify that the fundamental frequency phase angle readings are between the minimum and maximum readings listed in Table 4-4.

Table 4-4. Watts Performance, Line Frequency

Calibrator Output			Performance Limits							
Volts	Phase	Amps (mV)	W/kW		VA/kVA		VARs/kVARs		Phase	
			Min	Max	Min	Max	Min	Max	Min	Max
5.00	0.00	30.00	144	156	144	156	0	4	-2	2
8.00	0.00	30.00	233	247	233	247	0	4	-2	2
100.00	157.00	150.00	-14.3	-13.2	14.4	15.6	5.4	6.4	155	159
100.00	157.00	360.00	-37	-28	31	41	10	19	155	159
10.00	46.00	1300.00	8.5	9.6	12.4	13.6	8.8	9.9	44	48
100.00	46.00	1300.00	85	96	124	136	88	99	44	48

4-9. Testing Record Mode Performance

1. The equipment setup from the previous performance test, apply the last set of values from Table 4-4 to the Tester.
2. Press RECORD and then HOLD ENTER.

Examine Max., Avg., and Min. screens for correct readings according to Table 4-4.

Note

No VAR/KVAR in record mode.

4-10. Testing Memory Mode Performance (Model 41B Only)

1. Using the equipment setup from the previous performance test, apply the last set of values from Table 4-4 to the Tester.
2. Press MEMORY.
3. Using ◁ ▷ and HOLD ENTER, Clear, store, and recall the waveform in memory.

4-11. Testing Harmonics Volts Performance

Note

Make sure that the unit is set to "THD % RMS" before performing this procedure.

1. Press [key] until the harmonics screen is displayed on the Tester.
2. Press [V/A/W key] until V is displayed above the upper right corner of the harmonics display.
3. Press [V A Ø REF key] until A Ø is displayed in the top status line of the Tester.
4. Press SMOOTH until 20s is displayed in the top status line of the Tester.
5. Connect the calibrator NOTMAL output to the V and COM connectors on the Tester.
6. Connect the calubrator AUX output to the Current Probe connector on the Tester.
7. Set the calibrator output to 7.0V at 50 or 60 Hx on the NORMAL output and 700 mV at the same frequency on the AUX output. Press the WAVE MENUS softkey and ensure the phase angle is -10.0 degrees. Press the HARMONIC MENU softkey and ensure the HARMONIC selection is set to "1" and the FUNDMTL selection is set to "aux.", the Press OPR.
8. Move the Tester cursor to the corresponding harmonic number.
9. Verify that the harmonic amplitude and phase angle readings displayed by the Tester are within the minimum and maximum limits listed in Table 4-5.

Note

The polarity of the phase on the 5500A is always relative to the NORMAL channel output. Therefore,the Tester will read a positive phase when the 5500A output is a negative phase.

10. Repeat the previous three steps using the settings and limits in Table 4-5.

Table 4-5. Harmonics Performance for Volts

Fluke 5500A Output			Fluke Tester	Performance Limits			
Amplitude (V)	Harmonic No.	Phase (deg.)	Harmonic Cursor No.	Amplitude		Phase	
				Min	Max	Min	Max
7.00	1	-10.00	1	6.7	7.3	8	12
7.00	3	-20.00	3	6.7	7.3	14	26
7.00	9	-30.00	9	6.7	7.3	21	39
7.00	13	-40.00	13	6.7	7.3	29	51
7.00	21	-50.00	21	6.5	7.5	35	65
7.00	31	-60.00	31	6.2	7.8	40	80

4-12. Testing Harmonics Amps Performance

Note

Make sure that the unit is set to "THD % RMS" before performing this procedure.

1. Press [V A W] until A is displayed above the upper right corner of the harmonics display.
2. Press [V Ø A REF] until V Ø is displayed in the top status line of the Tester.
3. Press [SMOOTH] until ∿-20s is displayed in the top status line of the Tester.
4. Connect the calibrator NORMAL output to the V and COM connectors on the Tester.
5. Connect the calibrator AUX output to the Current Probe connector on the Tester
6. Set the calibrator output to 7.0 V at 50 or 60 Hz on the NORMAL output and 20 mV at the same frequency on the AUX output. Press the WAVE MENUS softkey and ensure the phase angle is 10.00 degrees. Press the HARMONIC MENU softkey and ensure the HARMONIC selection is set to "1" and the FUNDMTL selection is set to "normal", then press OPR.
7. Verify that the harmonic amplitude and phase angle readings displayed by the Tester are within the minimum and maximum limits listed in Table 4-6.

Table 4-6. Harmonics Performance for Amps

Fluke 5500A Output			Fluke Tester	Performance Limits			
Amplitude (mV)	Harmonic No.	Phase (deg.)	Harmonic Cursor No.	Amplitude		Phase	
				Min	Max	Min	Max
20.00	1	10.00	1	19.1	20.9	8	12
20.00	3	20.00	3	19.1	20.9	14	26
20.00	9	30.00	9	19.1	20.9	21	39
20.00	13	40.00	13	19.1	20.9	29	51
20.00	21	50.00	21	18.7	21.3	35	65
20.00	31	60.00	31	18.1	21.9	40	80

4-13. Testing Serial I/O Performance (Model 41B Only)

Confirming serial I/O performance requires the RS-232 optical interface cable, FlukeView™ software, and a PC running Window 3.1. If not already done, install the FlukeView™ software on the PC and configure for the appropriate serial port.

1. Connect the optical interface cable between the optical interface on the side of the Tester and the serial port of the PC.

Note

The correct serial port on the PC will be determined by the configuration of the PC and installation of the FlukeView™ software.

2. Open FlukeView™ software on the PC.
3. Turn on the Tester.
4. From the FlukeView™ toolbar, choose the camera icon.
5. Communication over the serial I/O port is confirmed when the picture window on the PC, displays a picture of the Tester's display with the appropriate values and/or waveform.
6. To confirm the print function, press the Print button and confirm the Tester displays "PRNT" in the upper left corner of the display and the following message appears:

```
* PRINTING *
PRESS ANY KEY TO STOP
```

7. To confirm the send function, press the Send button and confirm the Tester displays "SEND" in the upper left corner of the display. The same message appears as in step 6 above.

4-14. Calibrating the Tester

The Tester allows closed-case calibration using known reference sources. The meter automatically prompts you for the required reference signals, measures them, calculates the correction factors, and stores the correction factors in the nonvolatile calibration memory.

The Tester has a normal calibration cycle of 1 year. If the Tester fails the performance test or has been repaired, it should be calibrated. To meet the instrument specifications, listed in Chapter 1, the Tester should be calibrated with equipment meeting the minimum specifications given in Table 4-1.

4-15. Introduction

The Tester is calibrated using the calibration screen. Two factors are used to correct each a/d converter reading: offset and gain. AC voltages are used as inputs to both the offset and gain calculations. During the offset measurement, the instrument calculates the DC value of the AC input. This insures that the DC values reported, when AC is present, are correct.

$$CV = 2 \times [(Advalue \times GSF) + Offset]$$

CV is the calibrated value. *Advalue* is the present reading from the a/d converter. *GSF* is the gain scale factor and *Offset* is the value from the calibration sequence.

The basic calibration consists of sets of steps for Volts (banana jacks) and Amps (BNC inputs). Both inputs are calibrated using an AC Volt Reference Source.

Caution

Do not apply current sources to the Tester’s Clamp Probe (BNC) connector.

The entire calibration process must be completed before the new calibration factors can be stored in nonvolatile memory. If the calibration process is discontinued prior to completion, no changes are made to nonvolatile calibration memory.

4-16. Entering Calibration Mode

To put the Tester in the calibration mode and display the calibration screen, proceed as follows:

1. Allow the Tester to stabilize in an environment with an ambient temperature of 18 to 28 degrees Celsius and relative humidity of less than 70% for at least four hours.

Note

The Cal Enable switch is located in the battery compartment of the instrument beneath a calibration seal.

2. Remove the Tester’s battery access lid and batteries (Figure 4-2). Remove the calibration seal to reveal the calibration access hole.

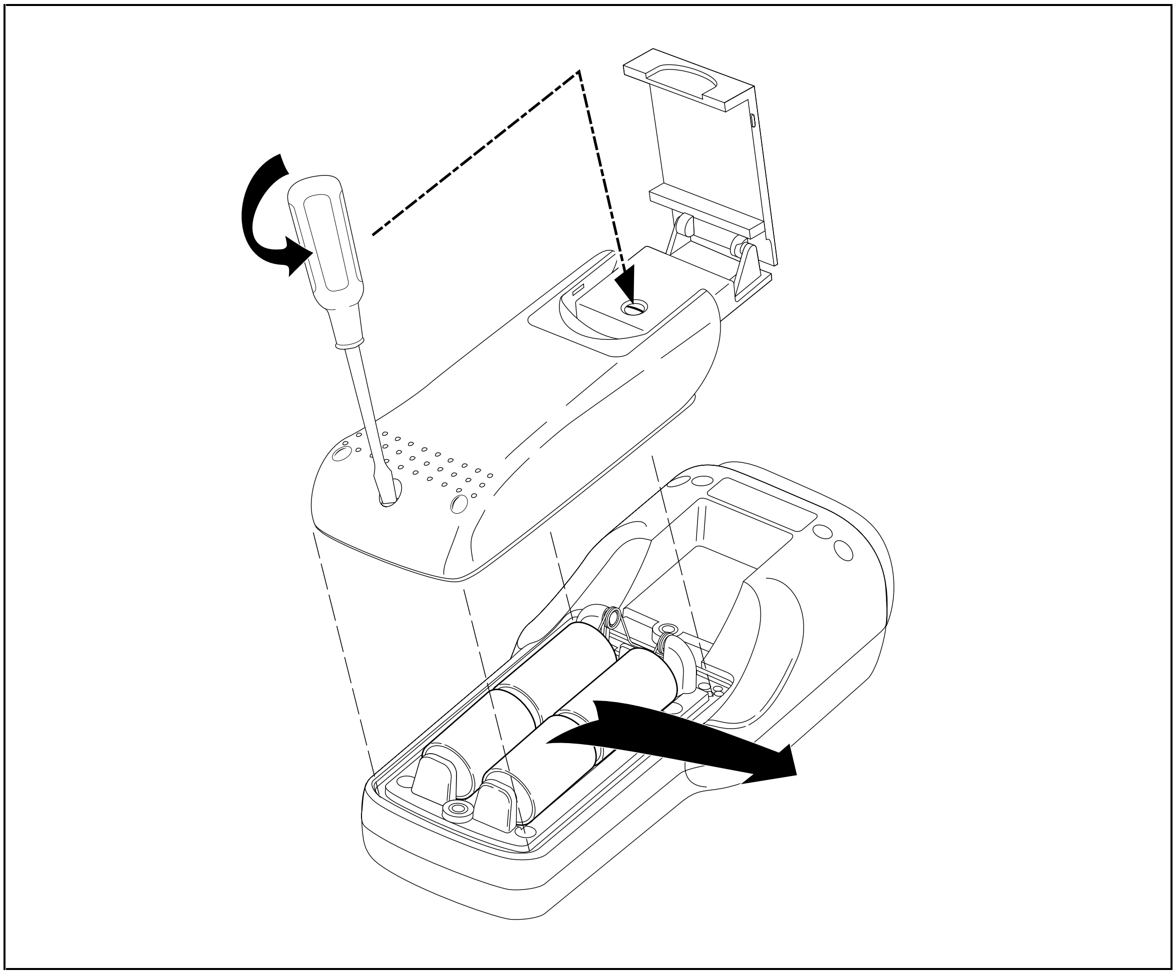


Figure 4-2. Battery Removal

3. In order for the Tester to remain on while replacing the battery door, remove the battery shunt spring and reinsert it with the spring's straight edge on the battery side of the plastic wall (Figure 4-3). Place four fresh "C" cell batteries in the Tester, taking care to ensure proper polarity.
4. Press [power key] to turn the Tester on and allow it to warm up for at least 2 minutes.

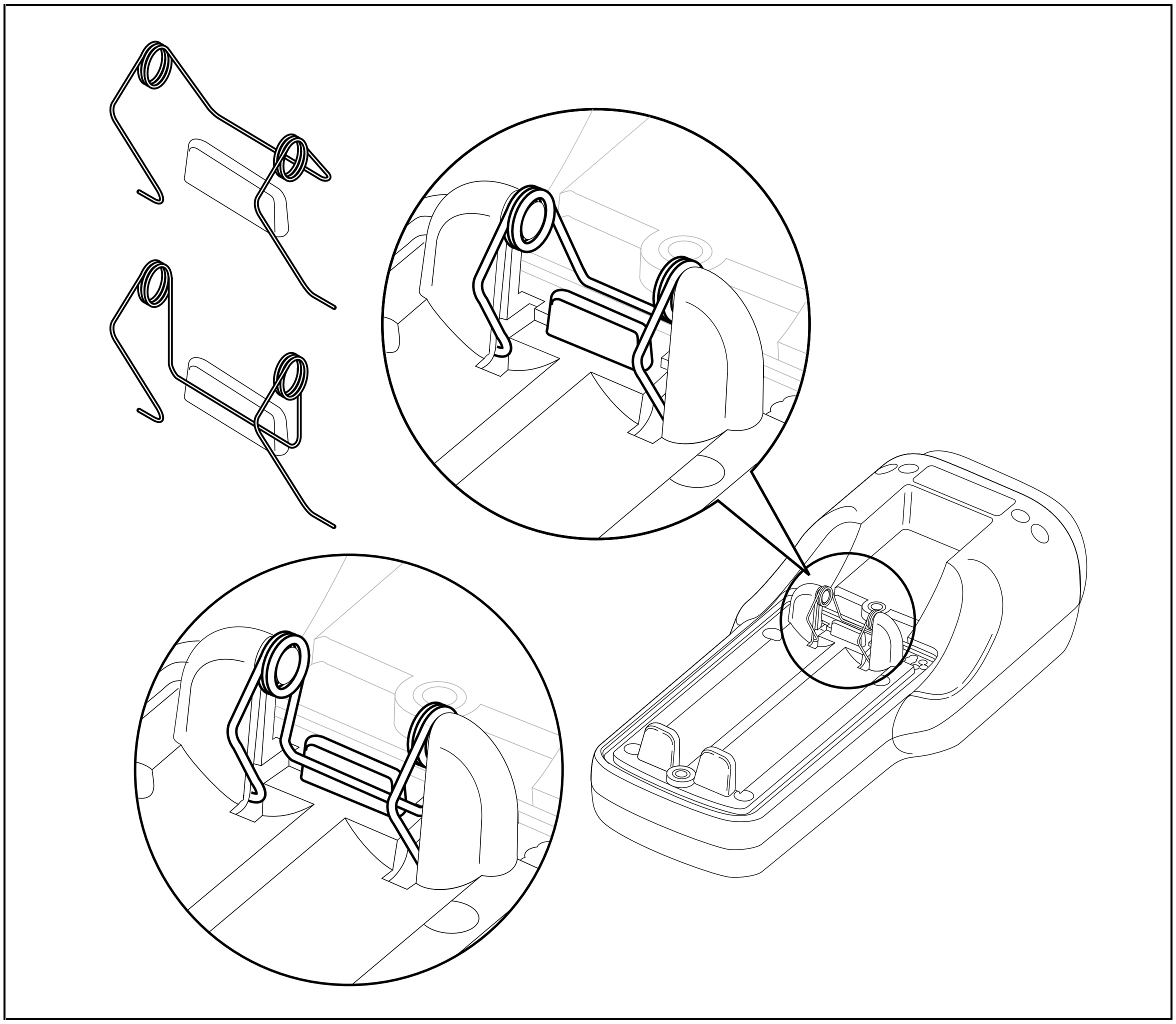


Figure 4-3. Battery Spring Adjustment

5. With the instrument in an upright position, the Cal Enable switch pads are in the largest and leftmost hole (Figure 4-4). Using a small flat-blade screwdriver or equivalent blunt-tipped conductive object, short together the two Cal Enable pads. The calibration mode is enabled when the Tester displays the "CAL AMP PROBE INPUT" menu and calibration factors. A command arrow, on the left of the display, should point to the APPLY VRMS instruction line.

Note

Contact bounce on the Cal Enable pads may advance the Cal Prompt beyond the 20A calibration range. In the event this happens, turn the Tester off then on and enable calibration again.

6. Reinstall the battery access lid on the instrument. See Figure 4-2.

The display also provides information for the RANGE that is being calibrated, the voltage to APPLY to the Tester inputs, and the resulting calibration FACTOR. All ranging is automatically taken care of by the Tester and only the calibration voltage needs to be supplied.

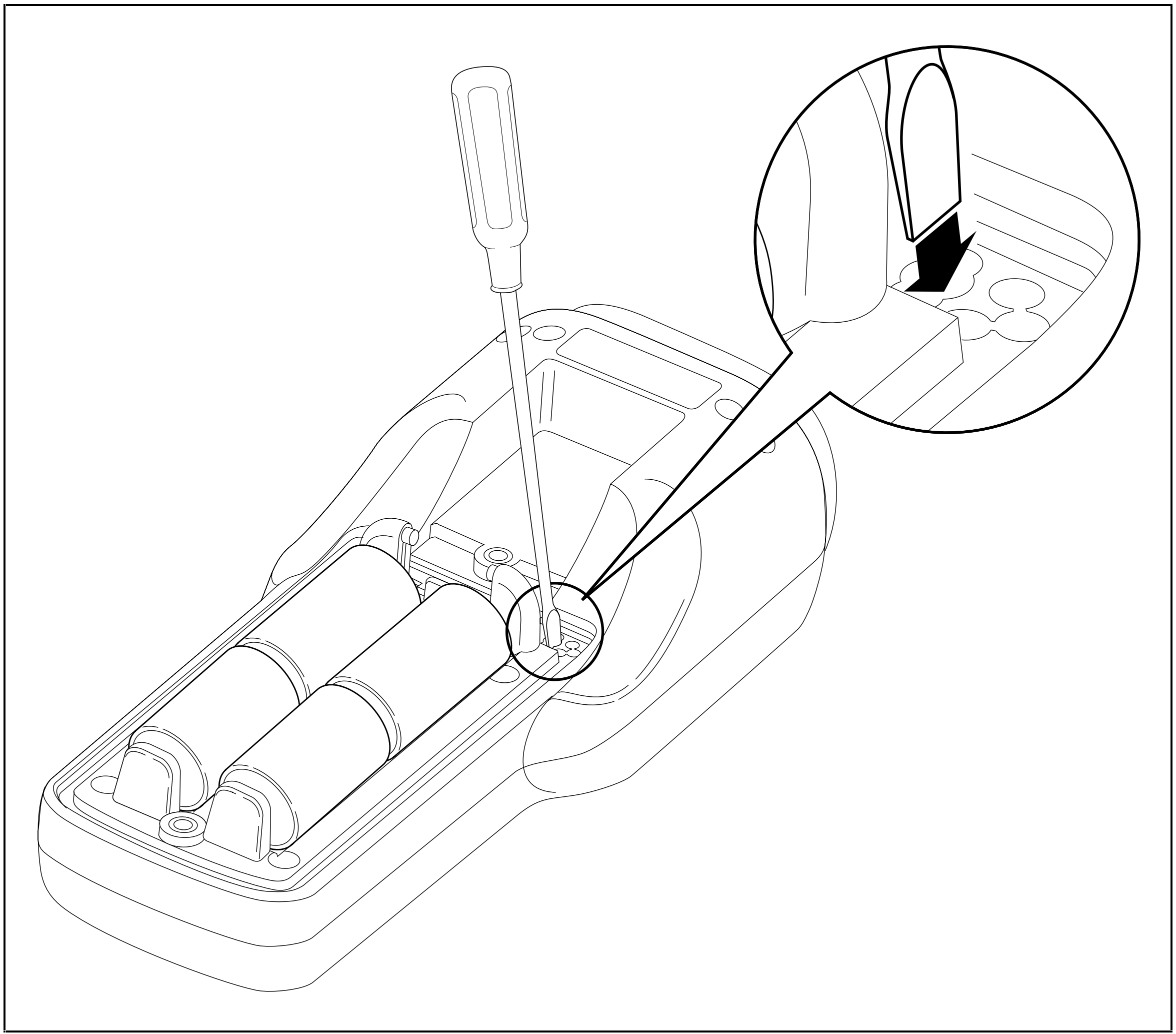


Figure 4-4. Calibration Access Hole

4-17. Making Calibration Adjustments

The calibration step being performed is identified by an arrow on the left side of the display. Each step calls for either a connection to be made or a known voltage applied to the input of the Tester. Pressing Enter will either move to the next step (in the case of an instruction) or store the displayed calibration factor for that specific test. By pressing the arrow key more than once, you can bypass a step in the calibration menu. When this happens you must restart the Calibration routine.

Note

Make sure each calibration step is complete before pressing enter. Press enter only once for each calibration step or instruction. There will be a slight delay before the arrow moves to the next prompt or instruction on the display after pressing enter.

Upon completion of all calibration steps, you are instructed to accept the Tester's new calibration factors by pressing [HOLD ENTER], or cancel the calibration by turning the Tester off. All other button operations are ignored.

To capture usable calibration factors, the calibration source output must be stable and the Tester factor readings must settle to their final value. Once the factor reading has stabilized, press [HOLD ENTER] to move to the next calibration step or instruction.

If all of the calibration steps are completed and ACCEPT CALIBRATION is performed by pressing [HOLD ENTER], the new calibration factors are stored in nonvolatile calibration memory. At this point, calibration is complete and the Tester exits the calibration mode.

While in the calibration mode, the Tester prompts you through the following steps:

Warning

During calibration, dangerous voltages are present in the instrument. To avoid shock, you must make sure the battery cover is installed.

1. Connect the calibrator HI and LO outputs to the Clamp Probe BNC connector on the Tester. Press [HOLD ENTER]. (A voltage source is used to calibrate the current input, DO NOT APPLY A CURRENT SOURCE TO THE BNC CONNECTOR.)
2. Apply 14 mV rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
3. Apply 140 mV rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
4. Apply 1.4V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
5. Press [HOLD ENTER] to start gain factor calibration.
6. Apply 14 mV rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
7. Apply 140 mV rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
8. Apply 1.4V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
9. Press [HOLD ENTER] to switch to the Voltage calibration display (The Tester displays "CAL VOLTS INPUT" for voltage calibration).

10. Disconnect the calibrator from the Clamp Probe BNC connector. Connect calibrator HI and LO outputs to the V and COM inputs of the Tester. Press [HOLD ENTER].

Warning

Dangerous voltages will be present on the calibration source and connecting cables during the following steps. Ensure that the calibrator is in standby mode before making any connection between the calibrator and Tester.

11. Apply 175V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
12. Apply 350V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
13. Apply 600V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
14. Press [HOLD ENTER] to start gain factor calibration.
15. Apply 175V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
16. Apply 350V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
17. Apply 600V rms at 60 Hz. After allowing the reading to settle, press [HOLD ENTER] on the Tester.
18. Press [HOLD ENTER] to accept calibration factors and store in nonvolatile calibration memory. The Tester will then return to normal operation.

Note

The CALIBRATION ERROR message will disappear after calibration is compete and power is cycled.

After calibrating the Tester, remove the battery access lid and batteries and return the battery shunt spring to its normal position. Place a new calibration seal (P/N 937045) over the calibration access port to prevent unintentional entry into the calibration mode. When the calibration seal is in place, install batteries and reinstall the battery access lid.

4-18. Exiting the Calibration Mode

Press [⏻] to exit the Calibration mode. If this button is pressed prior to completion of all calibration points, no changes are made to nonvolatile calibration memory.

4-19. Setting the Minimum Contrast Level

A minimum contrast level needs to be set whenever an LCD module, pca or the serial EEPROM (U22) is replaced. This setting provides a minimum useful level so that a user may not inadvertently set the screen blank.

1. Press [☼◑] to put the Tester in contrast mode.
2. Use [◁] or [▷] to set the display contrast to an optimum level (dark characters with light background).
3. Press and hold [☼◑] for at least 5 seconds. The contrast annunciator will turn off during the first second, turn on for 3 seconds along with the backlight, and then both will finally turn off. Release the contrast button.
4. Correct limit setting can be confirmed by changing the contrast to as light as possible (by pressing [☼◑] and holding [◁]).
5. Exit contrast mode normally.
6. Turn the Tester off and on.

The LCD contrast will be light but visible.

7. Return the Tester to optimum contrast.

Chapter 5
Troubleshooting

5-1. Introduction

This chapter describes troubleshooting procedures that can be used to isolate problems with the Tester. These procedures deal primarily with the digital section of the Tester. Due to the simplicity of the Analog section, only theory of operation is provided to support analog troubleshooting.

When troubleshooting the Tester, follow the precautions listed on the “Static Awareness” sheet to prevent damage from static discharge.

Signal names followed by “*” are active (asserted) low. Signal names not so marked are active high.

5-2. General Troubleshooting

Caution

To avoid contaminating the pca with oil from your fingers, handle the pca by its edges or wear gloves. A contaminated pca may not cause immediate instrument failure in controlled environments. Failures typically show up when contaminated units are operated in humid areas.

Before starting to troubleshoot, make sure the batteries are fresh enough to meet the minimum power supply voltages specified in Table 5-2.

5-3. Starting with a Dead Tester (Model 41B Only)

When the Tester is turned on, the display should flash dark and then come up in either the waveform, harmonics, or text screen mode. If it does not, it is possible that someone left the display contrast very low, causing the display to be blank. To eliminate this possibility, hold down [RECORD] while pressing [⓪] and then release both buttons.

If the Tester still appears dead, the problem could be in the power supplies or power-on circuit, the digital kernel, or the display module itself. Use the appropriate procedure below to isolate the problem.

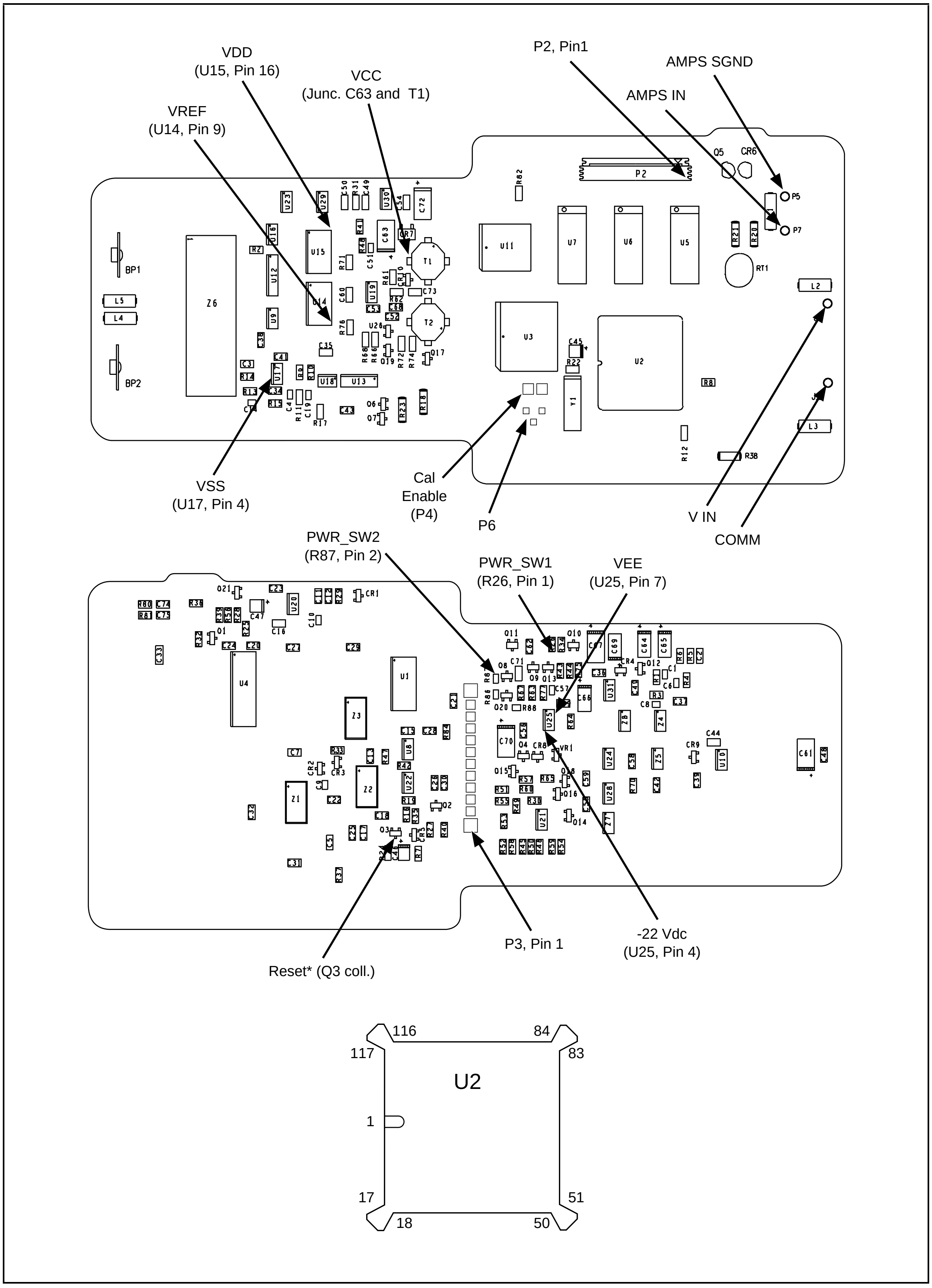


Figure 5-1. Test Point Locator

5-4. Troubleshooting the Power Supply

After pressing ⓞ, check the power supply voltages against the supply range values in Table 5-2.

If the power supplies do not come on, the problem could be with the power-on circuit itself. The following technique can be used to force the power supply on, even when the DSP or power-on circuit is defective. Refer to Figure 5-1 for test point locations in the following steps.

1. To ensure the Tester is not drawing too much current, remove the batteries and connect a 5-volt supply that indicates supply current between +VBT and -VBT.
2. Turn on the power supply.

   If the current draw with the Tester power off is greater than 0.5 mA, check the power supply capacitors C48 and C61 for shorts.
3. Short SW1 and SW2 together with a jumper while monitoring the amp meter on the supply. If the current draw exceeds the High Limit level in Table 5-1, immediately remove the power from the Tester and isolate the excessive current draw using appropriate troubleshooting methods.

Table 5-1. Power Supply Current Limits

Tester Condition	Low Limit	High Limit
Start-up Current	130 mA	200 mA
Normal w/o Backlight	70 mA	110 mA
Normal with Backlight	115 mA	165 mA

If the Tester powers up within the current limits of Table 5-1, you can check the power supply voltages against the voltage range specified in Table 5-2.

Table 5-2. Power Supplies

Supply Name	Measure		Supply Range
	From:	To:	
VCC	Jct. of C63 & T1	Comm	3.13V to 3.47V
VDD	U15-1	Comm	5.75 to 5.25V
VSS	U17-4	Comm	-7 to -5V
VEE	U25-7	Comm	-18.5 to -15V
VREF	U14-9	Comm	2.1016 to 2.1292V
-22 VDC	U25-4	Comm	-23.32 to -20.68V

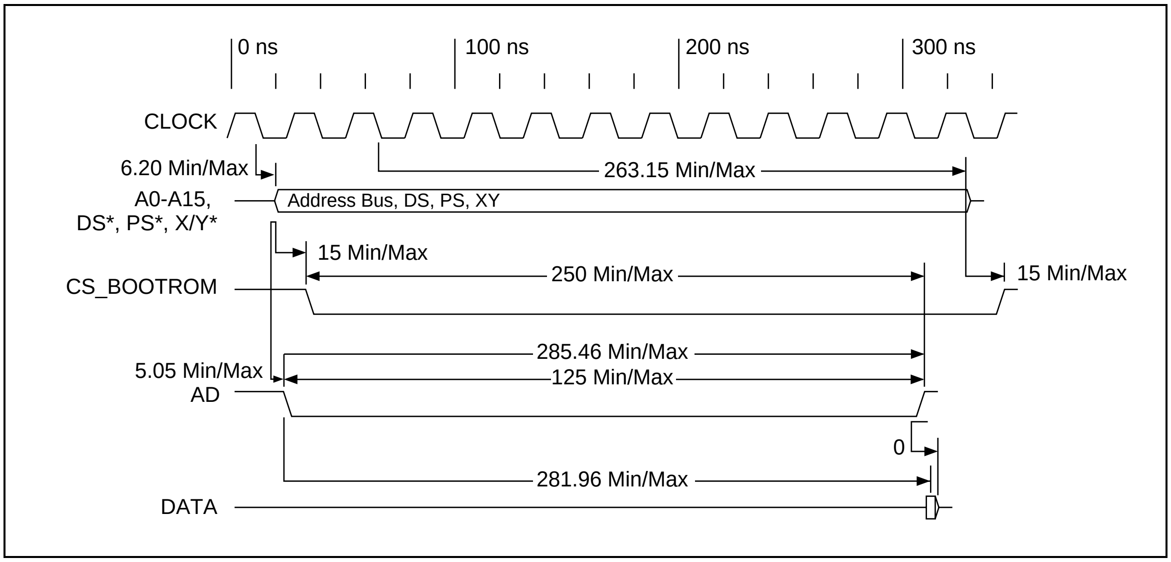
5-5. Troubleshooting the Digital Section

The digital section of the Tester is made up of the digital kernel, keypad, display, and optical interface. Fault isolation procedures for each of these areas are listed below.

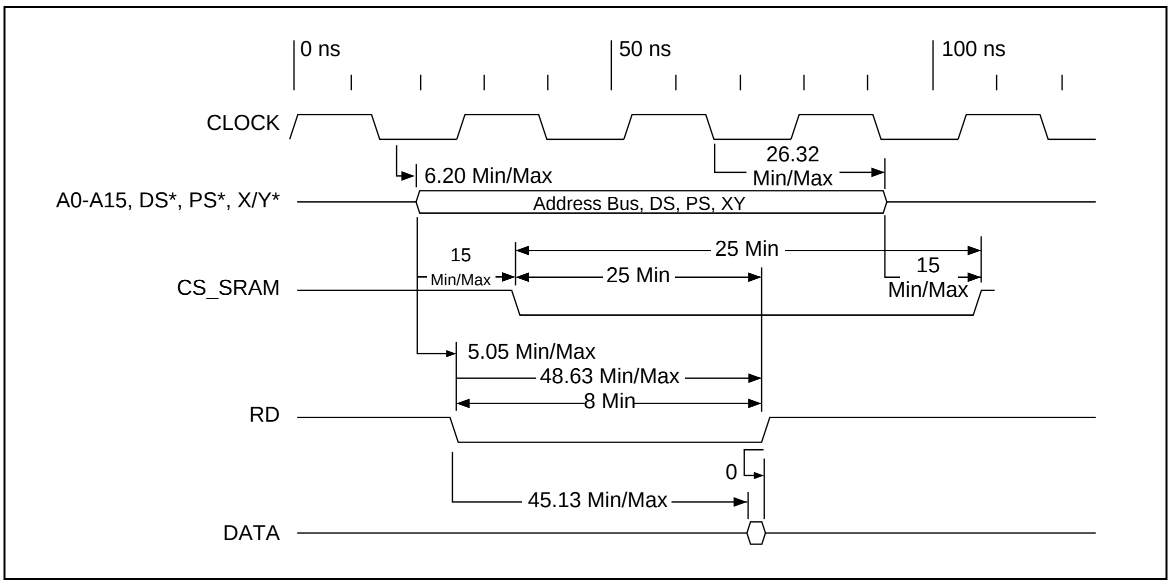
5-6. Troubleshooting the Digital Kernel

To isolate a problem within the Digital Kernel, proceed as follows:

1. Check for loose or unsoldered pins on U2 through U7.
2. Check all VCC pins on U2 for 3.3V. Because the VCC pins on the DSP supply power to different areas of the chip, any VCC pin that does not receive 3.3V when ⏻ is pressed could prevent the DSP from powering up.
3. Check that CKSUM_OK (U2-17) makes a transition from low to high in less than 150 ms when ⏻ is pressed or when the power supply is up to 3.3V. A checksum line that fails to make this transition indicates the program was not loaded properly from the EPROM into SRAM. This could indicate a problem with an address line, data line, control line (RD, WR, DS, PS, x/y) or EE_UPLOW line that is not high at reset, or it could indicate that U2 through U7 is faulty or has a bad solder joint.
4. Check that W_DOG (U2-35 or the side of C57 not tied to R77) changes state at least once every second. For certain areas of code, such as in the user interface, it may change state at a significantly higher rate. The minimum width of the a W_DOG pulse is 15µsec. If the W_DOG signal does not appear and the DSP is running with the CKSUM_OK line high, then U2 may be bad.
5. Check the DSP CLOCK signal (U2-123 or U3-43) with a high-speed oscilloscope. A clock frequency of 38.6918 MHz should be observed. If this clock signal is not present, verify that the oscillator circuit tied to U2-1 and U2-132 is correct. The crystal frequency is 3.86918 MHz. The DSP chip multiplies the crystal frequency by 10 to produce the DSP clock frequency.
6. The reset line (U2-125) should go high approximately 20 ms after the DSP chip sees 3.3V on its Vcc pins. If this does not occur, check the power supply and the reset circuit.
7. Check that MODE C (U2-119) is low when reset* (U2-125) goes from low to high. If it is not low, check that diode CR2 is correct and installed properly.
8. Check that MODE B (U2-120) is low when reset* (U2-125) goes from low to high. If it is not low, check that diode CR3 is correct and installed properly.
9. Check that MODE A (U2-121) is high when reset* (U2-125) goes from low to high. If it is not high, check that IRQA is pulled high and U3-9 is not driving IRQA low. If U3 is driving IRQA low when reset* is active, verify that the reset line to U3-2 is high when reset* is active. If U3-2 is high while reset* is active and U3 is still driving IRQA low, then U3 may be bad.
10. Check for activity on the CS_SRAM* and CS_BOOTROM* lines. When the DSP reset line is released, the DSP should start reading 1536 bytes starting at boot ROM address p:$C000. On power up, the DSP is set to 15 wait states for all memory locations; thus, CS_BOOTROM* is asserted low and should have a width of approximately 450 ns. Next, there should be a short pause (a few milliseconds) as the DSP executes the loaded code. Finally, the DSP copies all code from boot ROM to SRAM. Since the first 512 words of SRAM is onchip, no external SRAM activity will be observed until the onchip SRAM is full. While copying the remaining code to external SRAM, CS_BOOTROM* should be an active low pulse of approximately 310 ns when reading from the EPROM, and CS_SRAM* should be an active low pulse of approximately 70 ns when writing to external SRAM. The timing of the signals associated with reading the boot ROM or reading/writing to the SRAM should be compared with the following timing diagrams.



t16i.eps



t17i.eps

If these signals are not correct, verify that the appropriate signals (A15, A14, A5, A4, RD, WR, XY, PS) are present and correct. If these signals are not correct, you may have a problem with the DSP chip (U2). If these signals are correct, you may have a problem with U3.

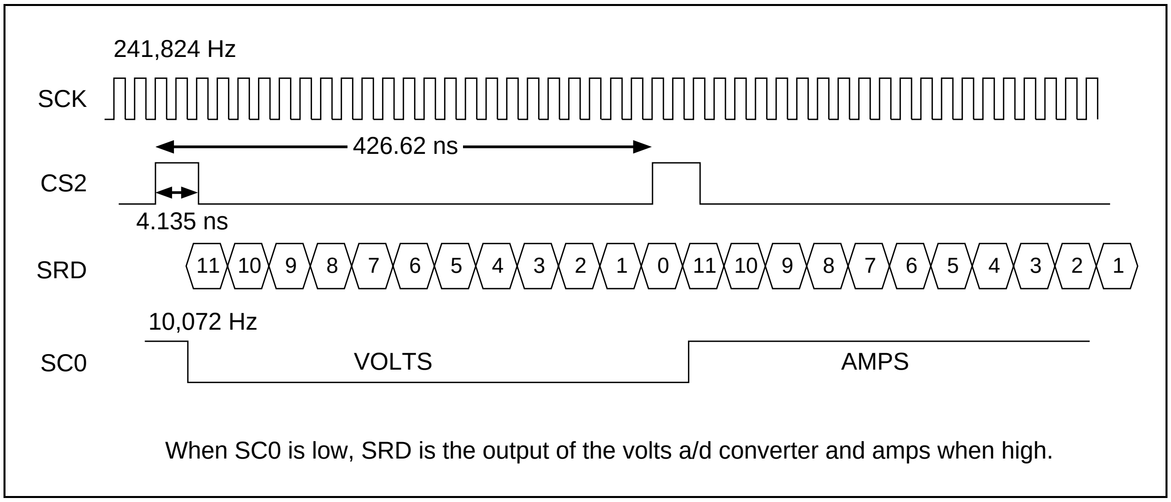
5-7. Troubleshooting the A/D Converter Output

To isolate a problem with the a/d converters, proceed as follows:

1. Check that SC0, SC2, SCK, and SRD at U2 are correct.
   - SC0 (U2-29) labeled ‘CHL’ - controls which A/D converter is being read.
   - SC2 (U2-32) labeled ‘FSO’ - Generates a one-bit pulse at the start of each A/D word, and it occurs at twice the sample rate of an A/D converter.
   - SCK (U2-31) labeled ‘SCK’ - Bit clock rate of the A/D converters.

- SRD (U2-38) labeled ‘DOUT’ - serial data received from the MUX in U3.

When the instrument is collecting data in normal operation mode, the above four waveforms can be observed with the following timing.



t18i.eps

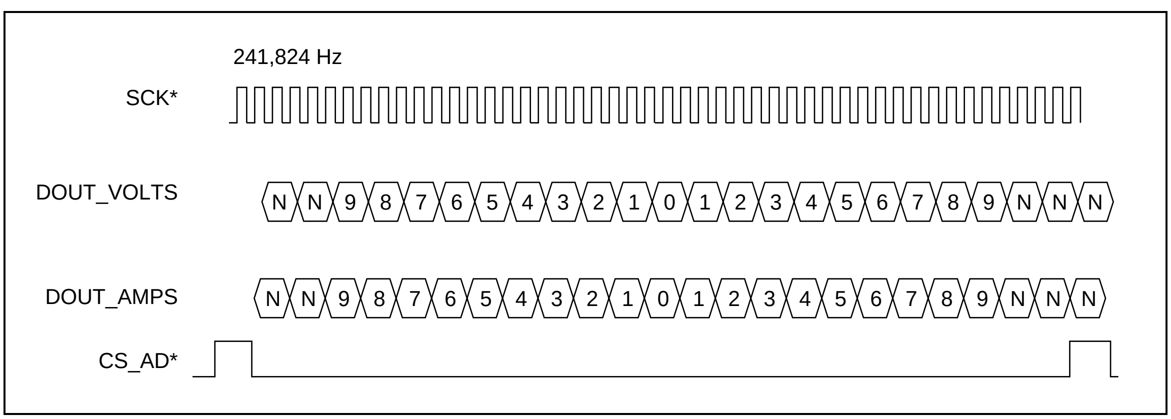
Note

When the instrument is in normal operation, it will collect data for about 234.6 ms when the input frequency is > ≈10Hz, then process data for ≈80 ms with the process repeating. With an input frequency <≈10Hz, it will collect data for 469.2 ms, then process data for ≈80 ms with the process repeating.

If SC0, SC2, and SCK are not present and the Tester is collecting data in normal operation (not in HOLD or memory mode), powering on properly, responding to key presses properly, and displaying the correct screen, the DSP (U2) may be defective.

If SRD is not correct, either the A/D converters may not be generating DOUT or U3 may not be producing the SRD signal correctly.

2. Check for proper communication between U3 and the A/Ds (U14 and U15). U3 has four control lines to the a/d converters:



r19i.eps

- SCK* (U14/U15-13 and U3-20) - A complemented version of SCK coming from the DSP chip.
- CS_AD* (U14/U15-1 and U3-17) - The chip select signal to the A/Ds which causes the A/Ds to sample and convert the result.
- DOUT_VOLTS (U15-12 or U3-13) - The serial data transmitted by the volts A/D converter.
- DOUT_AMPS (U14-12 or U3-11) - The serial data transmitted by the amps A/D converter.

Pins 13 and 11 on U3 should show a slightly attenuated version of pin 12 on U15 and U14. If this is not the case, verify that the 100Ω resistors (R71/R76) are correct.

When the instrument is collecting data in normal operation mode, the above four waveforms can be observed with the following timing.

If SCK* and CS_AD* are both correct and present at the A/D but the appropriate DOUT_VOLTS/DOUT_AMPS is not correct, there is some problem with the front end, possibly with the A/D converter itself.

The following problems may indicate a defective U3:

- MS 12 bits of DOUT_VOLTS followed by the MS 12 bits of DOUT_AMPS do not make it through U3 correctly.
- SC0 and SC2 (inputs to U3) are correct, but CS_AD* (output from U3) is not correct.
- SCK* is not an inverted version of SCK.

5-8. Troubleshooting the Keypad

To isolate a problem with the keypad, do the following:

1. Check the column (C0-C3) and row (R0-R3) lines that go to the keypad module. With no keys pressed and the instrument powered up, the PWR_SW1 (P3-10) should be at the battery voltage (5 to 6 volts). PWR_SW2 should be at digital ground. Column lines C0 to C3 should be driven low. Row lines R0 to R3 should be pulled high to VCC (3.3V). Thus, a key press should cause the appropriate row line to be driven low momentarily. Refer to the keyboard schematic in Chapter 7 to identify which row line will be driven low for a given key. If the column lines from the DSP chip (U2) are not low while the instrument is running and updating the display, the column line may be shorted to VCC or there may be a problem with the DSP chip. If a key press does not drive a row line low, there is probably a problem with the keypad or the elastomeric interconnect.
2. Check the IRQA* line while pressing a key. The IRQA line (U2-121 or U3-9) should be asserted low when a key is pressed to cause a user interface interrupt in the DSP chip (U2). If the IRQA line is asserted and the correct row line to the DSP chip is also asserted but the key still is not recognized, there may be a problem with the DSP chip.

   The IRQA* line should be asserted by U3 if the RESET line (U3-2) is low and one of the row line inputs to U3 is driven low by a key press. If the IRQA line is not driven low under these conditions, U3 may be defective.
3. Verify that after the interrupt has occurred, the appropriate row line is driven low when the appropriate column line is also driven low. This occurs during the interrupt process when the microprocessor is decoding the keypad. See the keypad schematic

in Chapter 7. If the row line is driven low for an incorrect column line, then there is some external problem, possibly a keypad or elastomeric interconnect problem.

5-9. Troubleshooting the Range Control Circuit

The Tester's measurement range can be changed manually or automatically. If the Tester is unable to change ranges, proceed with the following steps:

1. Check for the correct level at U1-12 through U1-18 by placing the instrument in manual range and verifying that the input latch is set to the values in Table 5-3.

Table 5-3. Latch Signals for Voltage Ranges

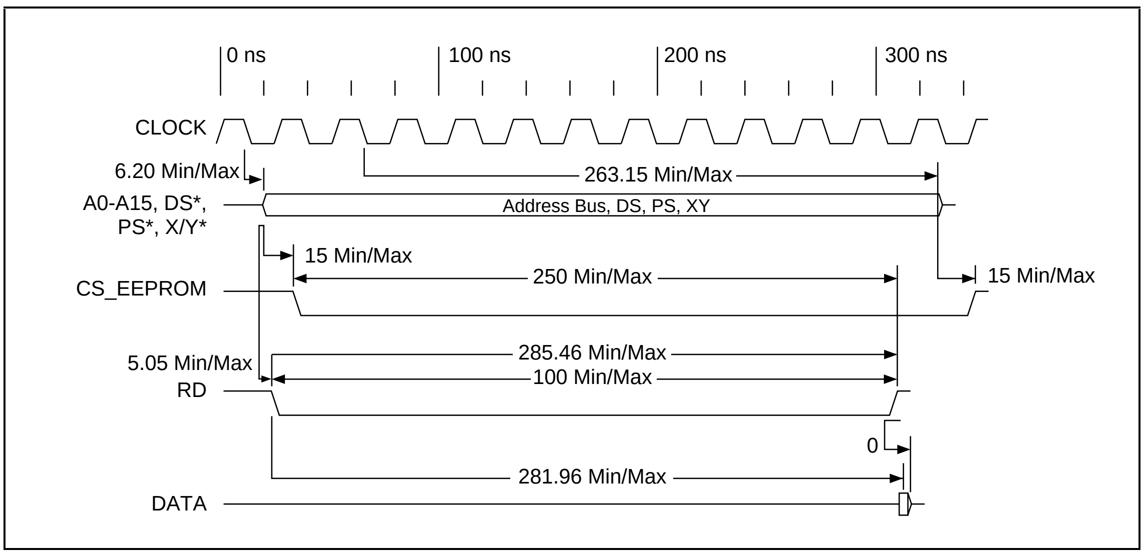
Range	U1-12	U1-13	U1-14	U1-15	U1-16	U1-17	U1-18
20V, 50V, 100V, and 200V	1	1	0	N/A	N/A	N/A	N/A
500V	1	0	1	N/A	N/A	N/A	N/A
1000V	0	1	1	N/A	N/A	N/A	N/A
2A, 5A, 10A, and 20A	N/A	N/A	N/A	1	0	1	0
50A, 100A, and 200A	N/A	N/A	N/A	1	0	0	1
500A, 1000A, and 2000A	N/A	N/A	N/A	0	1	0	1
"1" = Logic High (> 0.2V) and "0" = Logic Low (< 0.8V)							

2. If the latches are correctly written, there is a problem somewhere in the analog input circuits. Refer to the analog theory for troubleshooting assistance.
3. If latch (U1) is not written properly, verify that CS_GAIN* from U3-18 occurs when a range change is attempted. Also, the data should be on the appropriate latch input pins to be latched into the latch. If the CS_GAIN* pulse is not generated, verify that all of the correct signals are correctly feeding U3 (A15, A14, A5, A4, RD, WR, XY, PS). If they are correctly feeding, and you still do not have a correct CS_GAIN* signal, U3 may be defective. Alternatively, if the CS_GAIN* signal is present to the U1 latch but the correct data is not getting latched, verify that the data bus feeding the latch contains the correct data on the rising edge of the CS_GAIN* pulse. If the data bus does contain the correct data on the rising edge of CS_GAIN* but the data is not getting latched, there is probably a defective latch (U1).

5-10. Troubleshooting the EEPROM

The EEPROM (U11) is used for waveform storage and is only installed on the Model 41B. To isolate waveform storage problems, proceed with the following:

1. Verify that R82 and R84 are correct and installed. Also, verify that R83 and R85 are absent.
2. Verify that CS_EEPROM is changing states correctly when trying to read/write a waveform to EEPROM. The write timing to EEPROM should have similar timing with the RD signal replaced with the WR signal. If the CS_EEPROM* pulse is not generated, verify that all of the correct signals are present on U3 (A15, A14, A5, A4, RD, WR, XY, PS). If all signals are present and you still do not have a correct CS_EEPROM* signal, U3 may be defective.



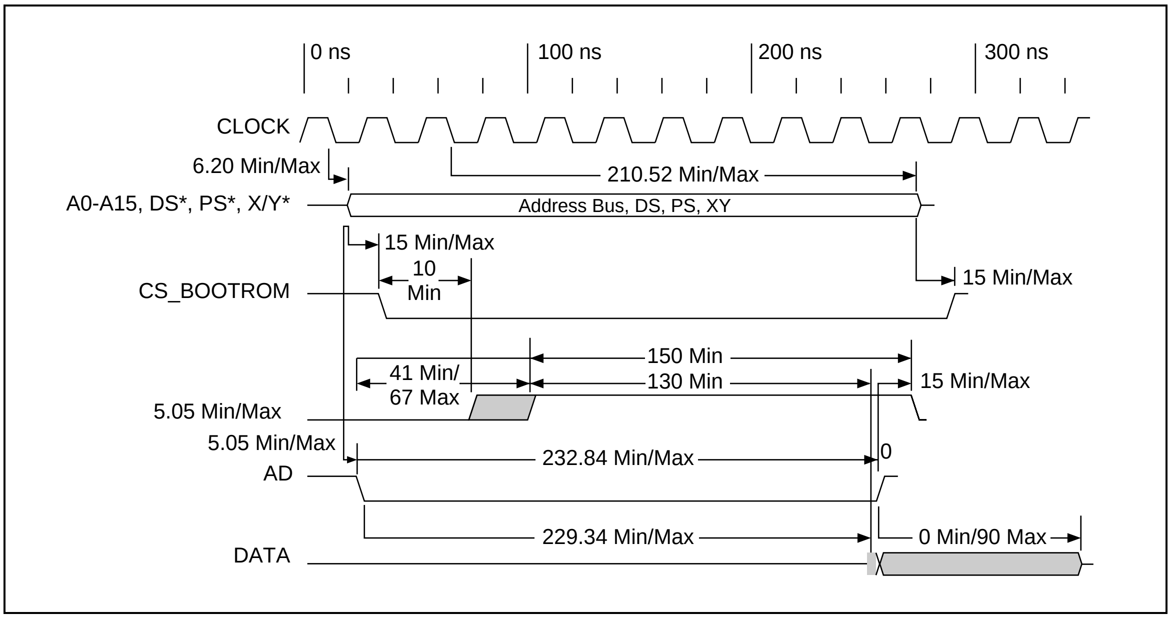
t20i.eps

3. Finally, if there are no solder problems with U11 (all address and data lines are properly connected), and the timing of the signals to U11 is correct, but the data written to U11 is not read back properly, U11 may be defective.

5-11. Troubleshooting the LCD Display Module

To isolate a problem when the LCD display appears dead, do the following:

1. First, verify that the display module is properly connected to the main circuit board. Make certain that the flex cable is not twisted or at an angle as it enters the molex connector of either the LCD module or the main circuit board.
2. Verify that the CS_LCD, and the LCD_E signals from U3 are correct. If the timing is correct, the problem may be with the contrast. If there are no connection problems, the timing waveforms are correct, and the contrast adjustment is not the problem (see “Starting with a Dead Tester” on page 1-3), there may be a problem with the LCD module.



t21i.eps

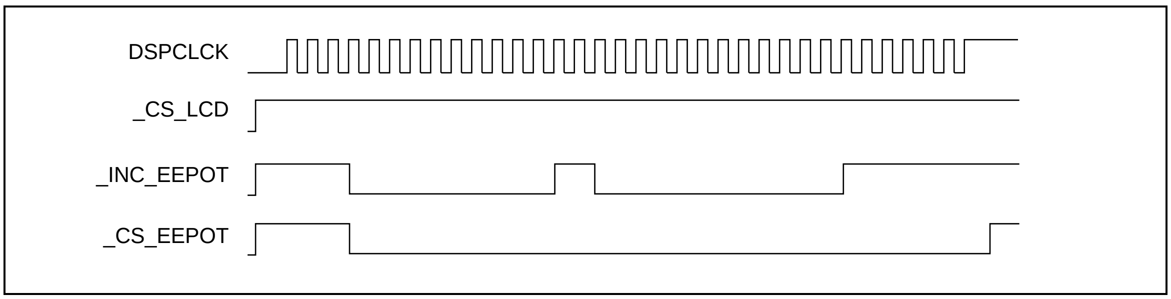
3. If the signals CS_LCD and LCD_E are not correct, verify that they are produced correctly by U3. When attempting to read and write to the display, the observed timing should match the LCD timing diagrams. If the inputs to U3 (A15, A14, A5, A4, RD, WR, XY, PS) are all present, there may be a problem with U3.

Vertical lines across the LCD screen will most likely be due to a misalignment of the LCD glass with its elastomeric connector. Replace the LCD display module to fix this problem.

To isolate a problem where the LCD display contrast does not adjust correctly, proceed as follows:

1. Press the arrow keys to verify that when entering contrast, the WIPER on the EEPOT (U8-5) can be moved between the top wiper voltage (U8-3) of ≈3.3V and the bottom wiper voltage (U8-6) of ≈0V. The right arrow moves the wiper toward the top wiper voltage or increases the contrast, and the left arrow moves the wiper toward the bottom wiper position or decreases the contrast. The newly selected value of contrast does not get saved unless you specifically exit the contrast feature by pressing [contrast key]. For example, if the Tester is in the contrast mode and you turn the power off, the contrast setting will not be saved as the new contrast of the display. If moving the WIPER through its range of values does not change the contrast of the display, there may be a problem with the analog contrast circuit or a problem with the LCD module.

2. Verify that U3 is producing the correct INC_EEPOT and CS_EEPOT signals as shown in the following timing diagram. EE_UPLOW (U8-2) controls the direction that the WIPER will move. CS_EEPOT (U8-7) selects the EEPOT. When the CS_EEPOT signal goes from low to high, thus deselecting the EEPOT, the present value of the EEPOT is saved to nonvolatile memory and will be used as EEPOT's default value upon receiving power. Once the EEPOT is selected, INC_EEPOT (U8-1) is pulsed low to increment/decrement the wiper position in accordance with the EE_UPLOW line. If the signals EE_UPLOW, CS_EEPOT, and INC_EEPOT are correct to U8, but the wiper does not move or the part does not save the result, U8 may be defective. If the CS_EEPOT or the INC_EEPOT* signals are not generated properly, verify that all the correct signals are present on U3. (A15, A14, A5, A4, RD, WR, XY, PS). If they are, U3 may be defective.



t22i.eps

5-12. Troubleshooting the Serial EEPROM

A faulty serial EEPROM is indicated if upon power-up, the Tester displays "CALIBRATION ERROR" or the contrast adjustment is not retained after the Tester has been calibrated and the power has been cycled off/on. To further isolate the problem, proceed as follows:

Note

During calibration, the CALIBRATION ERROR message will not disappear until power is cycled.

1. Display the power-up configuration screen by holding [HOLD ENTER] and pressing [⏻]. If multiple menu items are highlighted on a line or no menu items on a given line are highlighted, the serial EEPROM (U22) is probably faulty.

Note

In the next step, the Fluke 39 will not display the baud rate or printer type.

2. Reset the instrument to factory default by holding [RECORD] and pressing [⏻]. Then, power the Tester off and back on to bring up the power-up configuration screen. The following menu items should be highlighted: VOLT, WAVE, %RMS, 80I-500S, VOLT, 9.6K, and EPSON. If these menu items are not highlighted, the serial EEPROM (U22) may be defective.

Note

The serial EEPROM signals will be active just after the last step is completed in the power-up configuration screen.

3. When the serial EEPROM (U22) is read from or written to, the following conditions should be present:

- CS_EESER should be low (U22-1).

- SCK* line (U22-2) should be changing states at slightly less than a 500 KHz rate.
- Data written to the serial EEPROM (U22-3) should be the same as U2-33 (line labeled DIN).
- Data read from the serial EEPROM (U22-4) should be the same as the data supplied to the processor (U2-38).

  If the data on U22-4 and U2-38 are not the same, but the ATOD_EE (U3-12) is low, U3 may be defective.

Chapter 6
List of Replaceable Parts

6-1. Introduction

Chapter 6 contains an illustrated list of replaceable parts for the Fluke 39 Power Meter and 41B Power Harmonics Analyzer. Parts are listed by assembly; alphabetized by reference designator. Each assembly is accompanied by an illustration showing the location of each part and its reference designator. The parts lists give the following information:

- Reference designator
- An indication if the part is subject to damage by static discharge.
- Description
- Fluke stock number
- Total quantity.
- Any special notes (i.e., factory-selected part)

Caution

A * symbol indicates a device that may be damaged by static discharge.

6-2. How to Obtain Parts

Electrical parts may be ordered directly from the manufacturer by using the manufacturer’s part number, or from the Fluke Corporation and it authorized representatives by using the part number under the heading FLUKE STOCK NO. In the U.S., order directly from the Fluke Parts Dept. by calling 1-800-526-4731. Parts price information is available from the Fluke Corporation or its representatives. Prices are also available in a Fluke Replacement Parts Catalog which is available a request.

In the event that the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt delivery of the correct part, include the following information when you place an order:

- Instrument model and serial number
- Quantity
- Reference designator
- Part number and revision level of the pca containing the part.
- Description (as given under the DESCRIPTION heading)

6-3. Manual Status Information

The following Manual Status Information table defines the assembly revision levels that are documented in the manual. Revision levels are printed on the bottom side of each pca.

Manual Status Information

Ref Or Option Number	Assembly Name	Fluke Part Number	Revision Level
A1 (Fluke 39)	Main PCA	202820	A
A1 (Fluke 41B)	Main PCA	202827	A

6-4. Newer Instruments

Changes and improvements made to the instrument are identified be incrementing the revision letter marked on the affected pca. These changes are documented on a manual supplement sheet which, when applicable, is included with the manual.

6-5. Parts Lists

The following tables and figures list and illustrate the replaceable parts for the Tester.

Table 6-1. Fluke 39 Final Assembly

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
A1	* MAIN PCA	202820	1	
BT1-4	BATTERY,1.5V,0-480MA, ALKALINE SIZE C	423582	4	
H1	SCREW,PH,P,AM THD FORM,STL,4-14,.375	448456	4	
H20	SCREW,PH,P,AM THD FORM,STL,5-14,.812	942946	6	
J1	JUMPER, INPUT, RED	936877	1	
J2	JUMPER, INPUT, BLK	937040	1	
MP1	WINDOW, DECAL	202751	1	
MP2	CASE, TOP	104171	1	
MP3	LCD MODULE,160X128 GRAPH,TRNSFLECTIVE	928296	1	
MP4	MODULE, INPUT (OVERMOLDED)	202694	1	
MP5	CASE, BOTTOM (OVERMOLDED)	104182	1	
MP6	SUPPORT, INTERNAL	936815	1	
MP7	HOOK	202705	1	
MP8	SPRING, BATTERY	936906	1	
MP9	COVER, BATTERY (OVERMOLDED)	202702	1	
MP11	ACCESSORY PACK	936851	1	1
MP12	CLAMP,AC CURRENT	936943	1	
MP19	CONN,ELASTOMERIC,KEYPAD TO PWB,1.350L	942805	1	
MP26	SHOCK ABSORBER	948708	2	
MP27	SEAL, CALIBRATION	937045	1	
MP28	LABEL,ADHES,MYLAR,1.50,.312	943407	1	
S1	MODULE, KEYPAD	202788	1	
TM1	39/41B USER MANUAL,ENG/FR/SP	107612	1	
TM2	39/41B USER MANUAL	107607	1	
TM3	39/41B USER MANUAL,ENG/GER/IT	107620	1	
TM4	80I-500S INSTRUCTION SHEET,ENG	936922	1	
TM5	80I-500S INSTRUCTION SHEET,SPAN	948534	1	
TM6	80I-500S INSTRUCTION SHEET,GER	948539	1	
TM7	80I-500S INSTRUCTION SHEET,FR	948542	1	
TM8	39/41B QUICK REF GUIDE	107653	1	
W1	CABLE,FLAT,JUMPER,24COND,.039SP,1.30	936992	1	
XBT1, XBT2	CONTACT, BATTERY	936752	2	

NOTES:
1. ACCESSORY PACK INCLUDES THE FOLLOWING ITEMS:

MP1 - TEST LEAD,SI,R/A-STRT,BANANA,RED,TL24 - 927798 - 1
MP2 - TEST LEAD,SI,R/A-STRT,BANANA,BLK,TL24 - 927793 - 1
MP3 - PROBE,TEST,BANANA JACK,RED,TP20 - 927777 - 1
MP4 - PROBE,TEST,BANANA JACK,BLK,TP20 - 927772 - 1
MP5 - CLIP,ALLIGATOR,BANANA,SAFETY,RED,AC20 - 927582 - 1
MP6 - CLIP,ALLIGATOR,BANANA,SAFETY,BLK,AC20 - 927579 - 1

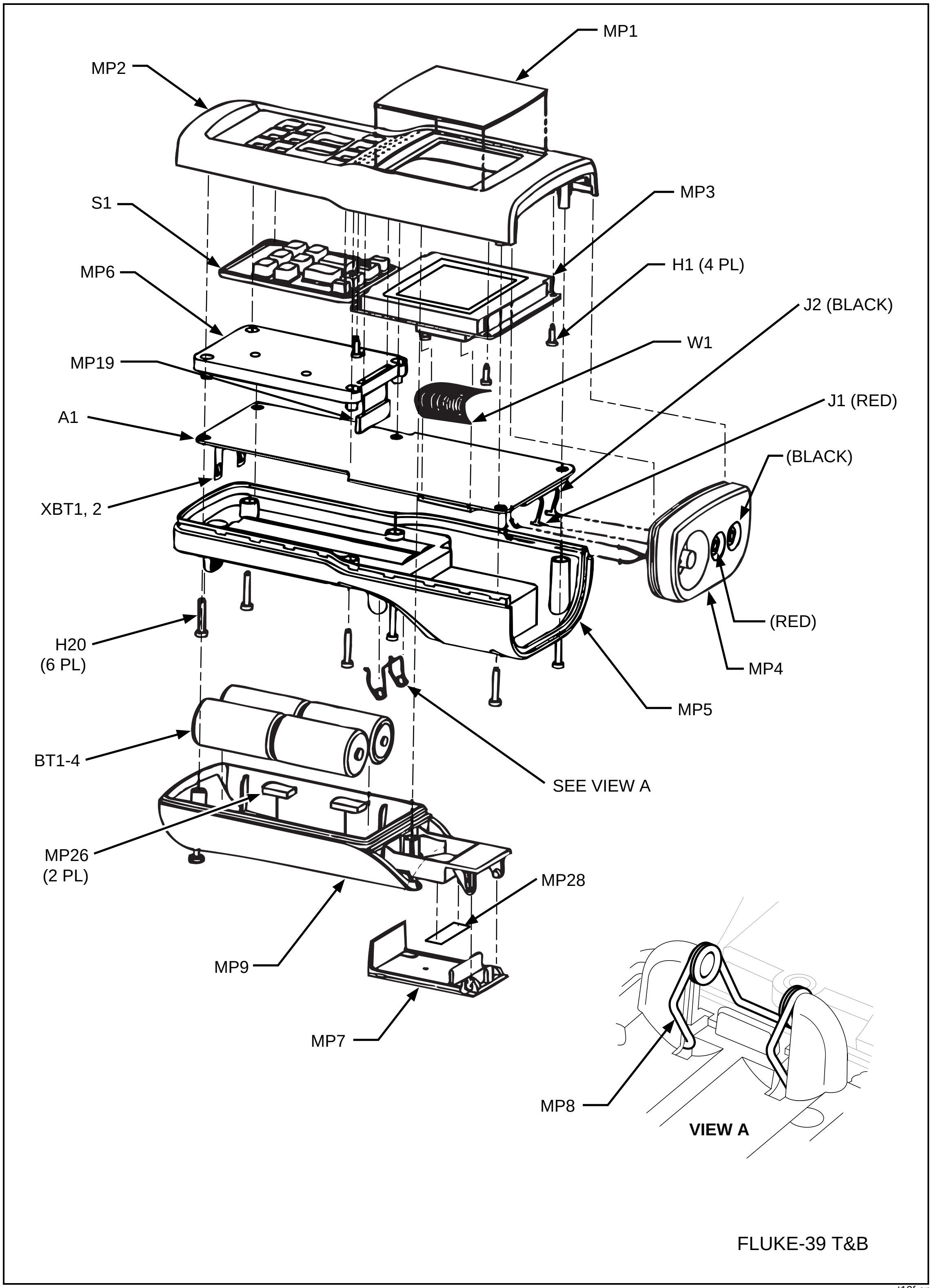


Figure 6-1. Fluke 39 Final Assembly

Table 6-2. Fluke 39 A1 Main PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1, C6		CAP,CER,750PF,+-1%,50V,C0G,0805	867643	2	
C2		CAP,CER,1000PF,+-1%,50V,C0G,1206	867668	1	
C3, C73		CAP,CER,1000PF,+-1%,50V,C0G,1206	867668	2	
C4		CAP,CER,100PF,+-1%,50V,C0G,0805	867650	1	
C5, C7, C13,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	30	
C15, C16, C18,			747287		
C20-24, C26-32,			747287		
C36, C37, C39,			747287		
C40, C42, C44,			747287		
C48, C55, C56,			747287		
C58, C59, C62			747287		
C8		CAP,CER,100PF,+-1%,50V,C0G,0805	867650	1	
C9		CAP,CER,8200PF,+-20%,50V,X7R,0805	942516	1	
C14, C19		CAP,CER,750PF,+-1%,50V,C0G,0805	867643	2	
C17, C25		CAP,CER,20PF,+-10%,50V,C0G,1206	747345	2	
C33		CAP,CER,47PF,+-10%,1000V,C0G,1808	930235	1	
C34, C35, C38,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	8	
C41, C43, C50,			747287		
C54, C60			747287		
C45		CAP,TA,1UF,+-20%,35V,3528	866970	1	
C46, C47		CAP,TA,1UF,+-20%,35V,3528	866970	2	
C49, C53		CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	2	
C51		CAP,CER,330PF,+-5%,50V,C0G,0805	512038	1	
C52, C68		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	2	
C57		CAP,CER,0.015UF,+-20%,50V,X7R,0805	493916	1	
C61, C67, C70		CAP,TA,100UF,+-20%,10V,7343	929877	3	
C63, C72		CAP,TA,220UF,+-20%,6V,7343H	944496	2	
C64-66, C69		CAP,TA,10UF,+-20%,16V,6032	867572	4	
C71		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	1	
C74		CAP,CER,470PF,+-10%,50V,C0G,1206	747360	1	
C75		CAP,CER,47PF,+-10%,50V,C0G,1206	747352	1	
CR2, CR3	*	DIODE,SI,SCHOTTKY,30V,SOT-23	930060	2	
CR4	*	DIODE,SI,SCHOTTKY,DUAL,30V,SOT-23	929745	1	
CR5, CR8, CR9	*	DIODE,SI,BV=70V,IO=50MA,DUAL,SOT-23	742320	3	
CR7	*	DIODE,SI,30 PIV,1.1 AMPS,SCHOTTKY	782573	1	
CR10	*	DIODE,SI,BV=75V,IO=250MA,SOT-23	830489	1	
L1-5		FERRITE CHIP,60 OHM @100 MHZ,1806	944645	5	
P2		CONN,FLAT FLEX,1MM CTR,RT ANG,24 POS	929893	1	

Table 6-2. Fluke 39 A1 Main PCA (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
P5,P7		SOCKET,SINGLE,PWB,FOR 0.026-0.033 PIN	811539	2	
Q2, Q3, Q13-15	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	912469	5	
Q4, Q9, Q12	*	TRANSISTOR,SI,N-DMOS FET,SOT-23	927538	3	
Q6,Q7	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742676	2	
Q8	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT	742676	1	
Q10	*	TRANSISTOR,SI,P-MOS,60V,SOT-23	867606	1	
Q11	*	TRANSISTOR,SI,NPN,BIASED,SC-59	942912	1	
Q16, Q18, Q20	*	TRANSISTOR,SI,PNP,50V,0.2W,SOT-23	820910	3	
Q17, Q19	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	912469	2	
R1, R5, R30, R51		RES,CERM,20K,+-5%,.125W,200PPM,1206	746644 746644	4	
R2, R10		RES,CERM,75K,+-1%,.125W,100PPM,1206	867085	2	
R3		RES,CERM,121K,+-1%,.125W,100PPM,1206	867437	1	
R4		RES,CERM,36.5K,+-1%,.125W,100PPM,1206	929906	1	
R6		RES,CERM,226K,+-1%,.125W,100PPM,1206	876524	1	
R7, R44		RES,CERM,36K,+-5%,.125W,200PPM,1206	769281	2	
R8, R12		RES,CERM,15K,+-5%,.125W,200PPM,1206	746628	2	
R9, R14		RES,CERM,20K,+-5%,.125W,200PPM,1206	746644	2	
R11		RES,CERM,121K,+-1%,.125W,100PPM,1206	867437	1	
R13		RES,CERM,36.5K,+-1%,.125W,100PPM,1206	929906	1	
R15		RES,CERM,226K,+-1%,.125W,100PPM,1206	876524	1	
R16, R34, R35, R40, R55, R60, R63		RES,CERM,100K,+-5%,.125W,200PPM,1206	740548 740548 740548	7	
R17, R66		RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	2	
R18, R23, R38		RES,CERM,470,+-1%,1W,100PPM,MELF	944244	3	
R19, R24, R75		RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	3	
R20, R21		RES,CERM,499K,+-1%,1W,100PPM,MELF	929922	2	
R22		RES,CERM,680K,+-5%,.125W,200PPM,1206	929901	1	
R26		RES,CERM,6.2K,+-5%,.125W,200PPM,1206	746016	1	
R27		RES,CERM,1K,+-5%,.125W,200PPM,1206	745992	1	
R28, R45		RES,CERM,1K,+-1%,.125W,100PPM,1206	783241	2	
R31		RES,CERM,510K,+-5%,.125W,200PPM,1206	746800	1	
R37		RES,CERM,47K,+-5%,.125W,200PPM,1206	746685	1	
R41		RES,CERM,10.5K,+-1%,.125W,100PPM,1206	851852	1	
R42		RES,CERM,200,+-1%,.125W,100PPM,1206	772798	1	
R43		RES,CERM,27K,+-5%,.125W,200PPM,1206	740530	1	
R46		RES,CERM,620K,+-5%,.125W,200PPM,1206	811919	1	

Table 6-2. Fluke 39 A1 Main PCA (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
R47		RES,CERM,6.98K,+-1%,.125W,100PPM,1206	929919	1	
R48		RES,CERM,17.8K,+-1%,.125W,100PPM,1206	929930	1	
R49		RES,CERM,24.9K,+-1%,.125W,100PPM,1206	867689	1	
R50		RES,CERM,29.4K,+-1%,.125W,100PPM,1206	929935	1	
R52		RES,CERM,37.4K,+-1%,.125W,100PPM,1206	867486	1	
R53		RES,CERM,20K,+-1%,.125W,100PPM,1206	927421	1	
R54		RES,CERM,3.3,+-5%,.125W,400PPM,1206	867502	1	
R57		RES,CERM,220K,+-5%,.125W,200PPM,1206	746750	1	
R58		RES,CERM,1M,+-1%,.125W,100PPM,1206	836387	1	
R59, R80		RES,CERM,10,+-5%,.125W,200PPM,1206	746214	2	
R61		RES,CERM,12.1K,+-1%,.125W,100PPM,1206	930032	1	
R62		RES,CERM,2.74K,+-1%,.125W,100PPM,1206	930156	1	
R64		RES,CERM,205K,+-1%,.125W,100PPM,1206	769836	1	
R65		RES,CERM,215K,+-1%,.125W,100PPM,1206	836643	1	
R67		RES,CERM,15M,+-5%,.125W,300PPM,1206	811968	1	
R68		RES,CERM,4.7K,+-5%,.125W,200PPM,120	740522		
R69		RES,CERM,10.5K,+-1%,.125W,100PPM,1206	851852	1	
R70		RES,CERM,0,+.05 MAX,.125W,1206	810747	1	
R71, R76		RES,CERM,100,+-5%,.125W,200PPM,1206	746297	2	
R72		RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	1	
R74		RES,CERM,36K,+-5%,.125W,200PPM,1206	769281	1	
R77		RES,CERM,220,+-5%,.125W,200PPM,1206	746347	1	
R81		RES,CERM,47,+-5%,.125W,200PPM,1206	746263	1	
R86, R87		RES,CERM,49.9K,+-1%,0.1W,100PPM,0805	928697	2	
R88		RES,CERM,12.1,+-1%,0.1W,100PPM,0805	930081	1	
RT1		THERMISTOR,POS,1.1K,+-20%,25 C	867192	1	
T1		INDUCTOR,100UH,+-20%,0.51ADC	929729	1	
T2		INDUCTOR,200UH,+-20%,0.36ADC	929732	1	
U1	*	IC,CMOS,OCTAL D F/F,+EDG,W/3 ST,SOIC	929869	1	
U2	*	IC,DIGITAL SIGNAL PROC,LV,24 BIT,PQFP	929740	1	
U3	*	LOGIC DEVICE PROGRAMMED	202801	1	
U4	*	EPROM, PROGRAMMED	202804	1	
U5-7	*	IC,CMOS,SRAM,32K X 8,LO V,25 NS,SOJ28	929799	3	
U8	*	IC,CMOS,EEPOT,1K OHM,32 TAPS,LO V,SO8	929786	1	
U9	*	IC,OP AMP,FET,PREC,LOW PWR,SNGL S,SO8	929828	1	
U10, U24	*	IC,OP AMP,FET,PREC,LOW PWR,SNGL S,SO8	929828	2	
U12, U13	*	IC,CMOS,QUAD BILATERAL SWITCH,SOIC	875232	2	
U14, U15	*	IC,CMOS,10 BIT A/D W/SAMPLE HOLD,SOIC	929070	2	

Table 6-2. Fluke 39 A1 Main PCA (cont)

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
U16-18	* IC,OP AMP,DUAL,PICOAMP IB,SO8	910836	3	
U19	* IC,CMOS,TIMER,LOW POWER,SO8	930151	1	
U21, U25	* IC,OP AMP,DUAL,LOW POWER,SOIC	867932	2	
U22	* IC,EEPROM,SERIAL,64 X 16,LO V,SO8	929802	1	
U23	* IC,+5V TO -5V CONVERTER,SWTCH CAP,SO8	929844	1	
U26	* IC,V REF,SHUNT,1.2 V,2%,150 PPM,SOT23	929489	1	
U28	* IC,VOLTAGE REF,2.5V,+-0.4%,25PPM,SO8	929831	1	
U29	* IC,V CONVERTER,CHARGE PUMP,100 MA,SO8	929851	1	
U30	* IC,VOLT REG,PWM,STEP-DOWN,ADJ,SO8	942953	1	
U31	* IC,VOLT REG,FIXED,+5V,UPOWR,LO DO,SO8	929190	1	
VR1	ZENER,UNCOMP,22V,5%,5.6MA,0.2W,SOT-23	831230	1	
Y1	CRYSTAL,3.86918MHZ,50PPM,SURFACE MT	929716	1	
Z1, Z3	RES,CERM,SOIC,14 PIN,13 RES,47K,+-2%	929864	2	
Z2	RES,CERM,SOIC,14 PIN,13 RES,30K,+-2%	930003	1	
Z4, Z8	RES,MF,SOIC,8 PIN,4 RES,2K,+-1%	929963	2	
Z5, Z7	RES,MF,SOIC,8 PIN,4 RES,CUSTOM	929968	2	
Z6	RNET, CERM, CUSTOM, HI V INST AMP	900576	1	

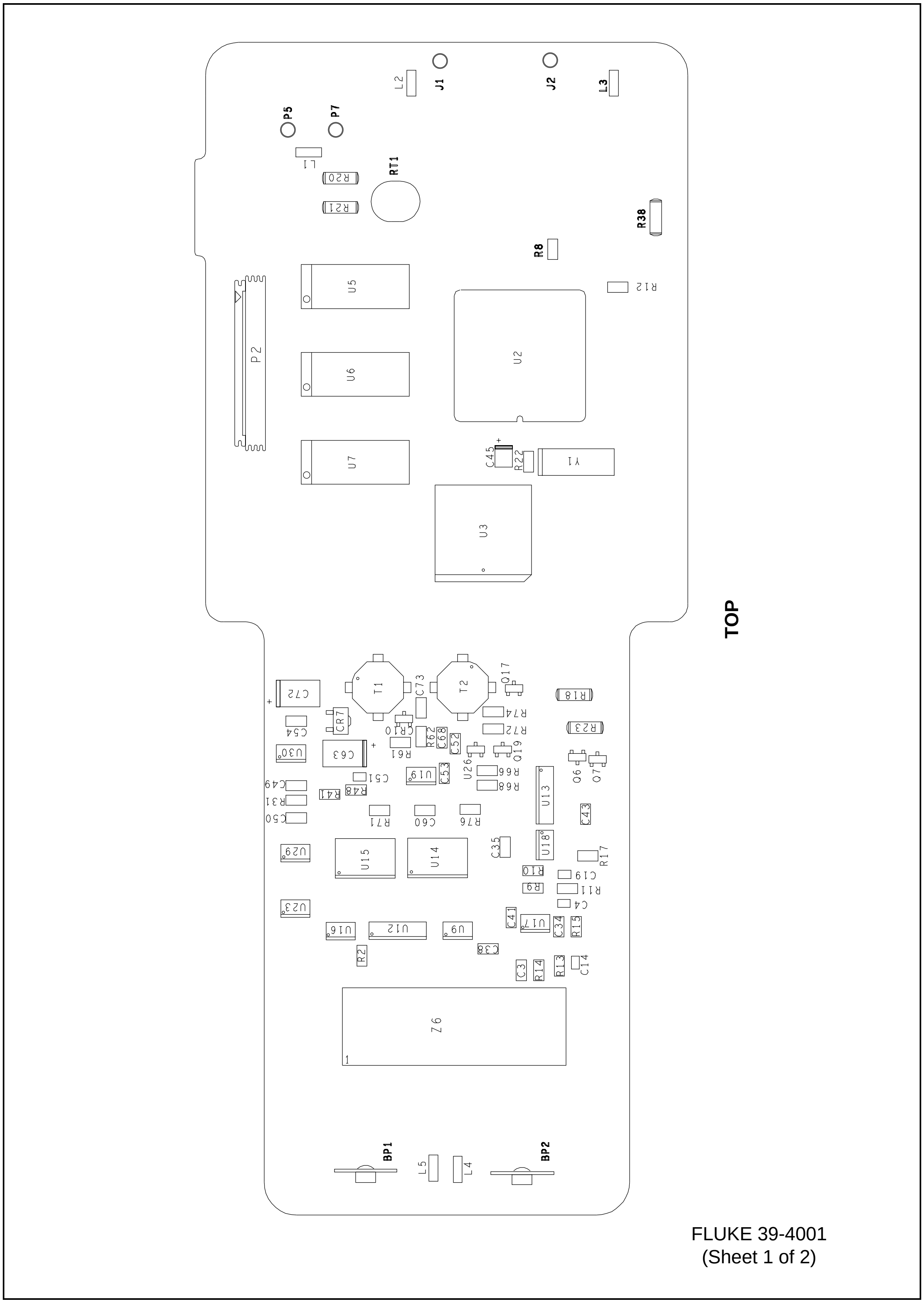


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Figure 6-2. Fluke 39 A1 Main PCA

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Figure 6-2. Fluke 39 A1 Main PCA (cont)

Table 6-3. Fluke 41B Final Assembly

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
A1	* MAIN PCA	202827	1	
BT1-4	BATTERY,1.5V,0-480MA, ALKALINE SIZE C	423582	4	
H1	SCREW,PH,P,AM THD FORM,STL,4-14,.375	448456	4	
H21	SCREW,PH,P,AM THD FORM,STL,5-14,.812	942946	6	
J1	JUMPER, INPUT, RED	936877	1	
J2	JUMPER, INPUT, BLK	937040	1	
MP1	WINDOW, DECAL	202744	1	
MP2	CASE, TOP	936828	1	
MP3	LCD MODULE,160X128 GRAPH,TRNSFLECTIVE	928296	1	
MP4	MODULE, INPUT (OVERMOLDED)	936836	1	
MP5	SUPPORT, INTERNAL	936815	1	
MP10	INSERT, CONTAINER	936729	1	
MP6	CASE, BOTTOM (OVERMOLDED)	936831	1	
MP7	HOOK	936810	1	
MP8	SPRING, BATTERY	936906	1	
MP9	COVER, BATTERY (OVERMOLDED)	936807	1	
MP11	ACCESSORY PACK	936851	1	1
MP12	ACCESSORY PACK, RS232	936856	1	2
MP13	CLAMP,AC CURRENT	936943	1	
MP19	HOLDER,LED	937011	1	
MP20	CONN,ELASTOMERIC,KEYPAD TO PWB,1.350L	942805	1	
MP27	SHOCK ABSORBER	948708	2	
MP31	SEAL, CALIBRATION	937045	1	
MP32	LABEL,ADHES,MYLAR,1.50,.312	943407	1	
MP37	CONTAINER TOP	202777	1	
MP40	SOFTWARE, FLUKEVIEW 41	936880	1	
S1	MODULE, KEYPAD	936745	1	
TM1	39/41B USER MANUAL	107607	1	
TM2	39/41B USER MANUAL,ENG/FR/SP	107612	1	
TM3	39/41B USER MANUAL,ENG/GER/IT	107620	1	
TM4	80I-500S INSTRUCTION SHEET,ENG	936922	1	
TM5	80I-500S INSTRUCTION SHEET,SPAN	948534	1	
TM6	80I-500S INSTRUCTION SHEET,GER	948539	1	
TM7	80I-500S INSTRUCTION SHEET,FR	948542	1	
TM8	39/41B QUICK REF GUIDE	107653	1	
TM10	SW41 FLUKEVIEW SOFTWARE USERS MANUAL	107631	1	
TM11	SW41 FLUKEVIEW SOFTWARE USERS MANUAL,INTL	600855	1	

Table 6-3. Fluke 41B Final Assembly (cont)

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
W1	CABLE,FLAT,JUMPER,24COND,.039SP,1.30	936992	1	
XBT1, XBT2	CONTACT, BATTERY	936752	2	

NOTES:

1. ACCESSORY PACK INCLUDES THE FOLLOWING ITEMS:

    MP1 - TEST LEAD,SI,R/A-STRT,BANANA,RED,TL24 - 927798 - 1

    MP2 - TEST LEAD,SI,R/A-STRT,BANANA,BLK,TL24 - 927793 - 1

    MP3 - PROBE,TEST,BANANA JACK,RED,TP20 - 927777 - 1

    MP4 - PROBE,TEST,BANANA JACK,BLK,TP20 - 927772 - 1

    MP5 - CLIP,ALLIGATOR,BANANA,SAFETY,RED,AC20 - 927582 - 1

    MP6 - CLIP,ALLIGATOR,BANANA,SAFETY,BLK,AC20 - 927579 - 1

2. ACCESSORY PACK RS232 INCLUDES THE FOLLOWING ITEMS:

    W1 - CABLE, RS232 - 936872 - 1

    CP1 - ADAPTER,D-SUB 9 PIN,KD-SUB 25 SCKT - 929187 - 1

    CP2 - ADAPTER,D-SUB 25 PIN,D-SUB 25 PIN - 867940 - 1

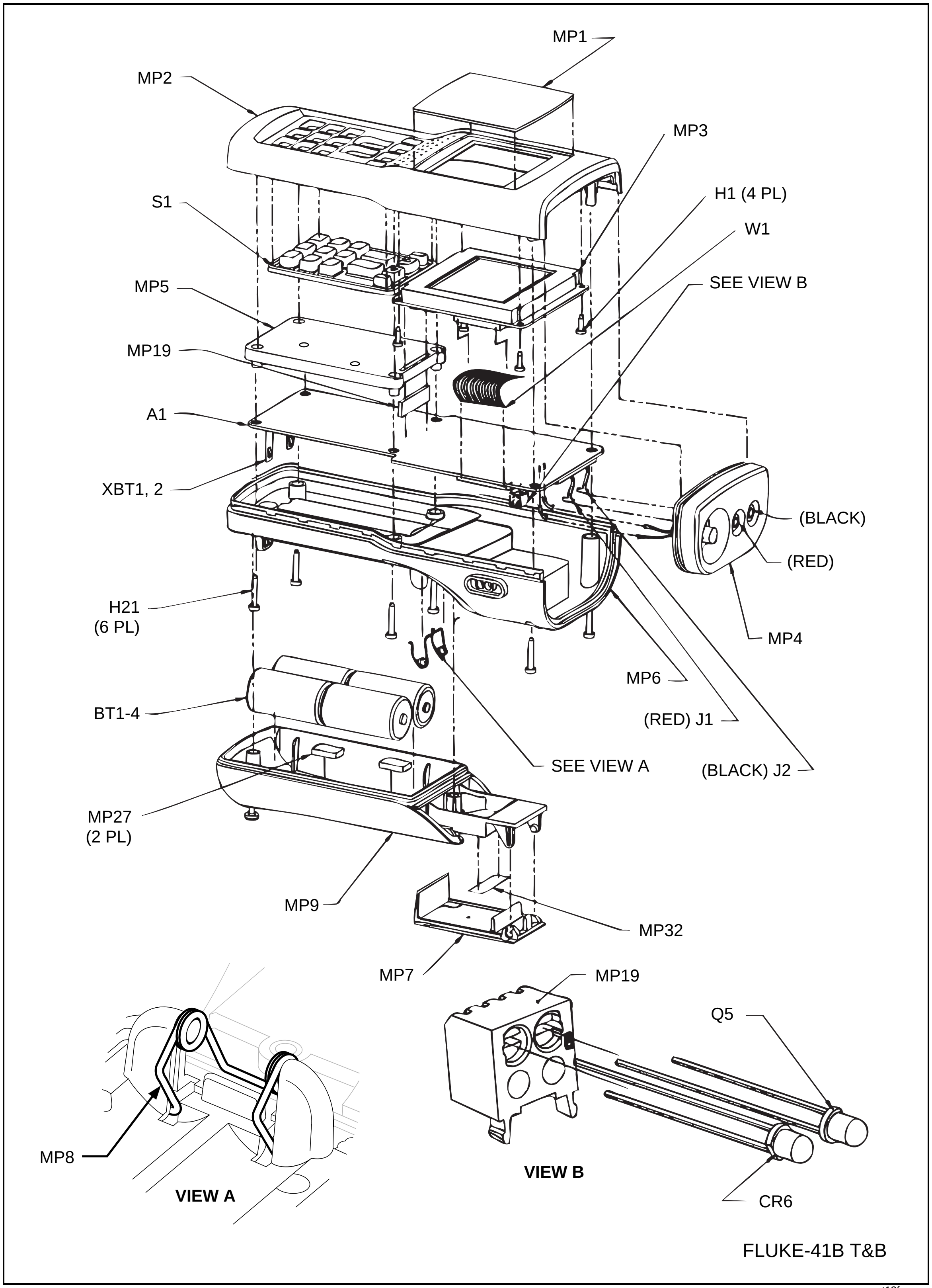

Figure 6-3. Fluke 41B Final Assembly

Table 6-4. Fluke 41B A1 Main PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1, C6		CAP,CER,750PF,+-1%,50V,C0G,0805	867643	2	
C2		CAP,CER,1000PF,+-1%,50V,C0G,1206	867668	1	
C3, C73		CAP,CER,1000PF,+-1%,50V,C0G,1206	867668	2	
C4		CAP,CER,100PF,+-1%,50V,C0G,0805	867650	1	
C5, C7, C13,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	30	
C15, C16, C18,			747287		
C20-24, C26-32,			747287		
C36, C37, C39,			747287		
C40, C42, C44,			747287		
C48, C55, C56,			747287		
C58, C59, C62			747287		
C8		CAP,CER,100PF,+-1%,50V,C0G,0805	867650	1	
C9		CAP,CER,8200PF,+-20%,50V,X7R,0805	942516	1	
C10		CAP,CER,2700PF,+-20%,50V,X7R,0805	930149	1	
C11, C12,C71		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	3	
C14, C19		CAP,CER,750PF,+-1%,50V,C0G,0805	867643	2	
C17, C25		CAP,CER,20PF,+-10%,50V,C0G,1206	747345	2	
C33		CAP,CER,47PF,+-10%,1000V,C0G,1808	930235	1	
C34, C35, C38,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	8	
C41, C43, C50,			747287		
C54, C60			747287		
C45		CAP,TA,1UF,+-20%,35V,3528	866970	1	
C46, C47		CAP,TA,1UF,+-20%,35V,3528	866970	2	
C49, C53		CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	2	
C51		CAP,CER,330PF,+-5%,50V,C0G,0805	512038	1	
C52, C68		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	2	
C57		CAP,CER,0.015UF,+-20%,50V,X7R,0805	493916	1	
C61, C67, C70		CAP,TA,100UF,+-20%,10V,7343	929877	3	
C63, C72		CAP,TA,220UF,+-20%,6V,7343H	944496	2	
C64-66, C69		CAP,TA,10UF,+-20%,16V,6032	867572	4	
C74		CAP,CER,470PF,+-10%,50V,C0G,1206	747360	1	
C75		CAP,CER,47PF,+-10%,50V,C0G,1206	747352	1	
CR1, CR5, CR8,	*	DIODE,SI,BV=70V,IO=50MA,DUAL,SOT-23	742320	4	
CR9	*		742320		
CR2, CR3	*	DIODE,SI,SCHOTTKY,30V,SOT-23	930060	2	
CR4	*	DIODE,SI,SCHOTTKY,DUAL,30V,SOT-23	929745	1	
CR6		LED,INFRA RED,T1,950 NM	942545	1	

Table 6-4. Fluke 41B A1 Main PCA (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
CR7	*	DIODE,SI,30 PIV,1.1 AMPS,SCHOTTKY	782573	1	
CR10	*	DIODE,SI,BV=75V,IO=250MA,SOT-23	830489	1	
L1-5		FERRITE CHIP,60 OHM @100 MHZ,1806	944645	5	
P2		CONN,FLAT FLEX,1MM CTR,RT ANG,24 POS	929893	1	
P5, P7		SOCKET,SINGLE,PWB,FOR 0.026-0.033 PIN	811539	2	
Q1, Q8	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742676	2	
Q2, Q3, Q13-15	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	912469	5	
Q4, Q9, Q12	*	TRANSISTOR,SI,N-DMOS FET,SOT-23	927538	3	
Q5	*	TRANSITOR,PHOTO,W/ DAYLIGHT FILTER	942540	1	
Q6, Q7	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742676	2	
Q10	*	TRANSISTOR,SI,P-MOS,60V,SOT-23	867606	1	
Q11	*	TRANSISTOR,SI,NPN,BIASED,SC-59	942912	1	
Q16, Q18, Q20	*	TRANSISTOR,SI,PNP,50V,0.2W,SOT-23	820910	3	
Q17, Q19	*	TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	912469	2	
Q21	*	TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742684	1	
R1, R5, R30,		RES,CERM,20K,+-5%,.125W,200PPM,1206	746644	4	
R51			746644		
R2, R10		RES,CERM,75K,+-1%,.125W,100PPM,1206	867085	2	
R3		RES,CERM,121K,+-1%,.125W,100PPM,1206	867437	1	
R4		RES,CERM,36.5K,+-1%,.125W,100PPM,1206	929906	1	
R6		RES,CERM,226K,+-1%,.125W,100PPM,1206	876524	1	
R7, R44		RES,CERM,36K,+-5%,.125W,200PPM,1206	769281	2	
R8, R12		RES,CERM,15K,+-5%,.125W,200PPM,1206	746628	2	
R9, R14		RES,CERM,20K,+-5%,.125W,200PPM,1206	746644	2	
R11		RES,CERM,121K,+-1%,.125W,100PPM,1206	867437	1	
R13		RES,CERM,36.5K,+-1%,.125W,100PPM,1206	929906	1	
R15		RES,CERM,226K,+-1%,.125W,100PPM,1206	876524	1	
R16, R34, R35,		RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	7	
R40, R55, R60,			740548		
R63			740548		
R17, R66		RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	2	
R18, R23, R38		RES,CERM,470,+-1%,1W,100PPM,MELF	944244	3	
R19, R24, R75		RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	3	
R20, R21		RES,CERM,499K,+-1%,1W,100PPM,MELF	929922	2	
R22		RES,CERM,680K,+-5%,.125W,200PPM,1206	929901	1	
R25		RES,CERM,11K,+-1%,.125W,100PPM,1206	867291	1	
R26		RES,CERM,6.2K,+-5%,.125W,200PPM,1206	746016	1	

Table 6-4. Fluke 41B A1 Main PCA (cont)

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
R27	RES,CERM,1K,+-5%,.125W,200PPM,1206	745992	1	
R28, R32, R45	RES,CERM,1K,+-1%,.125W,100PPM,1206	783241	3	
R29	RES,CERM,464K,+-1%,.125W,100PPM,1206	929898	1	
R31	RES,CERM,510K,+-5%,.125W,200PPM,1206	746800	1	
R33, R70, R84	RES,CERM,0,+.05 MAX,.125W,1206	810747	3	
R36	RES,CERM,150,+-1%,.125W,100PPM,1206	772780	1	
R37	RES,CERM,47K,+-5%,.125W,200PPM,1206	746685	1	
R39	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522	1	
R41	RES,CERM,10.5K,+-1%,.125W,100PPM,1206	851852	1	
R42	RES,CERM,200,+-1%,.125W,100PPM,1206	772798	1	
R43	RES,CERM,27K,+-5%,.125W,200PPM,1206	740530	1	
R46	RES,CERM,620K,+-5%,.125W,200PPM,1206	811919	1	
R47	RES,CERM,6.98K,+-1%,.125W,100PPM,1206	929919	1	
R48	RES,CERM,17.8K,+-1%,.125W,100PPM,1206	929930	1	
R49	RES,CERM,24.9K,+-1%,.125W,100PPM,1206	867689	1	
R50	RES,CERM,29.4K,+-1%,.125W,100PPM,1206	929935	1	
R52	RES,CERM,37.4K,+-1%,.125W,100PPM,1206	867486	1	
R53	RES,CERM,20K,+-1%,.125W,100PPM,1206	927421	1	
R54	RES,CERM,3.3,+-5%,.125W,400PPM,1206	867502	1	
R56	RES,CERM,1.33K,+-1%,.125W,100PPM,1206	801423	1	
R57	RES,CERM,220K,+-5%,.125W,200PPM,1206	746750	1	
R58	RES,CERM,1M,+-1%,.125W,100PPM,1206	836387	1	
R59, R80	RES,CERM,10,+-5%,.125W,200PPM,1206	746214	2	
R61	RES,CERM,12.1K,+-1%,.125W,100PPM,1206	930032	1	
R62	RES,CERM,2.74K,+-1%,.125W,100PPM,1206	930156	1	
R64	RES,CERM,205K,+-1%,.125W,100PPM,1206	769836	1	
R65	RES,CERM,215K,+-1%,.125W,100PPM,1206	836643	1	
R67	RES,CERM,15M,+-5%,.125W,300PPM,1206	811968	1	
R68	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522	1	
R69	RES,CERM,10.5K,+-1%,.125W,100PPM,1206	851852	1	
R71, R76	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	2	
R72	RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	1	
R74	RES,CERM,36K,+-5%,.125W,200PPM,1206	769281	1	
R77	RES,CERM,220,+-5%,.125W,200PPM,1206	746347	1	
R81	RES,CERM,47,+-5%,.125W,200PPM,1206	746263	1	
R82	RES,CERM,0,+.05 MAX,.125W,1206	810747	1	
R86, R87	RES,CERM,49.9K,+-1%,0.1W,100PPM,0805	928697	2	

Table 6-4. Fluke 41B A1 Main PCA (cont)

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
R88	RES,CERM,12.1,+-1%,0.1W,100PPM,0805	930081	1	
RT1	THERMISTOR,POS,1.1K,+-20%,25 C	867192	1	
T1	INDUCTOR,100UH,+-20%,0.51ADC	929729	1	
T2	INDUCTOR,200UH,+-20%,0.36ADC	929732	1	
U1	* IC,CMOS,OCTAL D F/F,+EDG,W/3 ST,SOIC	929869	1	
U2	* IC,DIGITAL SIGNAL PROC,LV,24 BIT,PQFP	929740	1	
U3	* LOGIC DEVICE PROGRAMMED	202801	1	
U4	* EPROM, PROGRAMMED	202804	1	
U5-7	* IC,CMOS,SRAM,32K X 8,LO V,25 NS,SOJ28	929799	3	
U8	* IC,CMOS,EEPOT,1K OHM,32 TAPS,LO V,SO8	929786	1	
U9	* IC,OP AMP,FET,PREC,LOW PWR,SNGL S,SO8	929828	1	
U10, U24	* IC,OP AMP,FET,PREC,LOW PWR,SNGL S,SO8	929828	2	
U11	* IC,CMOS,EEPROM,LV,32K X 8,250 NS,PLCC	929737	1	
U12, U13	* IC,CMOS,QUAD BILATERAL SWITCH,SOIC	875232	2	
U14, U15	* IC,CMOS,10 BIT A/D W/SAMPLE HOLD,SOIC	929070	2	
U16-18	* IC,OP AMP,DUAL,PICOAMP IB,SO8	910836	3	
U19	* IC,CMOS,TIMER,LOW POWER,SO8	930151	1	
U20, U21, U25	* IC,OP AMP,DUAL,LOW POWER,SOIC	867932	3	
U22	* IC,EEPROM,SERIAL,64 X 16,LO V,SO8	929802	1	
U23	* IC,+5V TO -5V CONVERTER,SWTCH CAP,SO8	929844	1	
U26	* IC,V REF,SHUNT,1.2 V,2%,150 PPM,SOT23	929489	1	
U28	* IC,VOLTAGE REF,2.5V,+-0.4%,25PPM,SO8	929831	1	
U29	* IC,V CONVERTER,CHARGE PUMP,100 MA,SO8	929851	1	
U30	* IC,VOLT REG,PWM,STEP-DOWN,ADJ,SO8	942953	1	
U31	* IC,VOLT REG,FIXED,+5V,UPOWR,LO DO,SO8	929190	1	
VR1	ZENER,UNCOMP,22V,5%,5.6MA,0.2W,SOT-23	831230	1	
Y1	CRYSTAL,3.86918MHZ,50PPM,SURFACE MT	929716	1	
Z1, Z3	RES,CERM,SOIC,14 PIN,13 RES,47K,+-2%	929864	2	
Z2	RES,CERM,SOIC,14 PIN,13 RES,30K,+-2%	930003	1	
Z4, Z8	RES,MF,SOIC,8 PIN,4 RES,2K,+-1%	929963	2	
Z5, Z7	RES,MF,SOIC,8 PIN,4 RES,CUSTOM	929968	2	
Z6	RNET, CERM, CUSTOM, HI V INST AMP	900576	1	

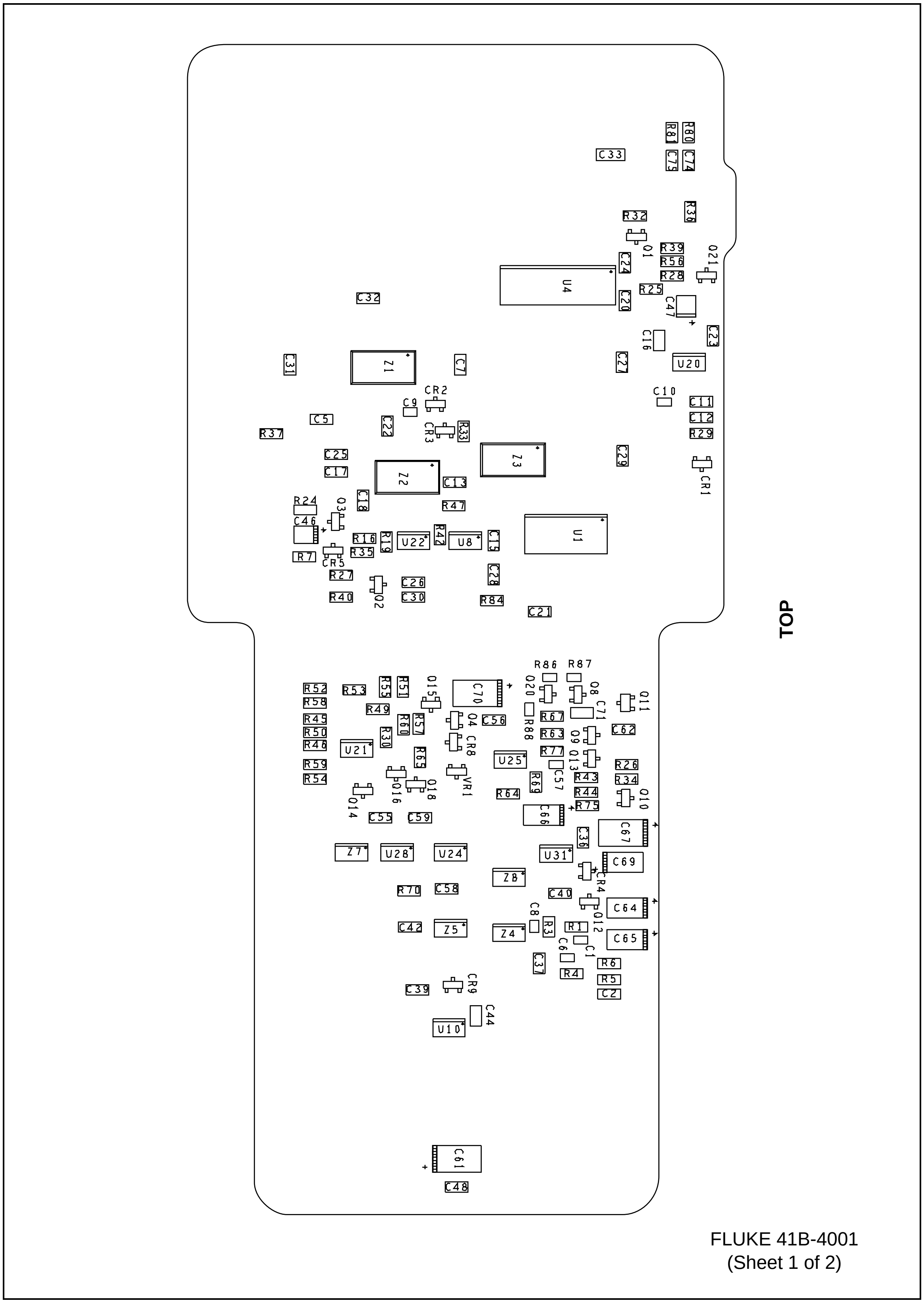

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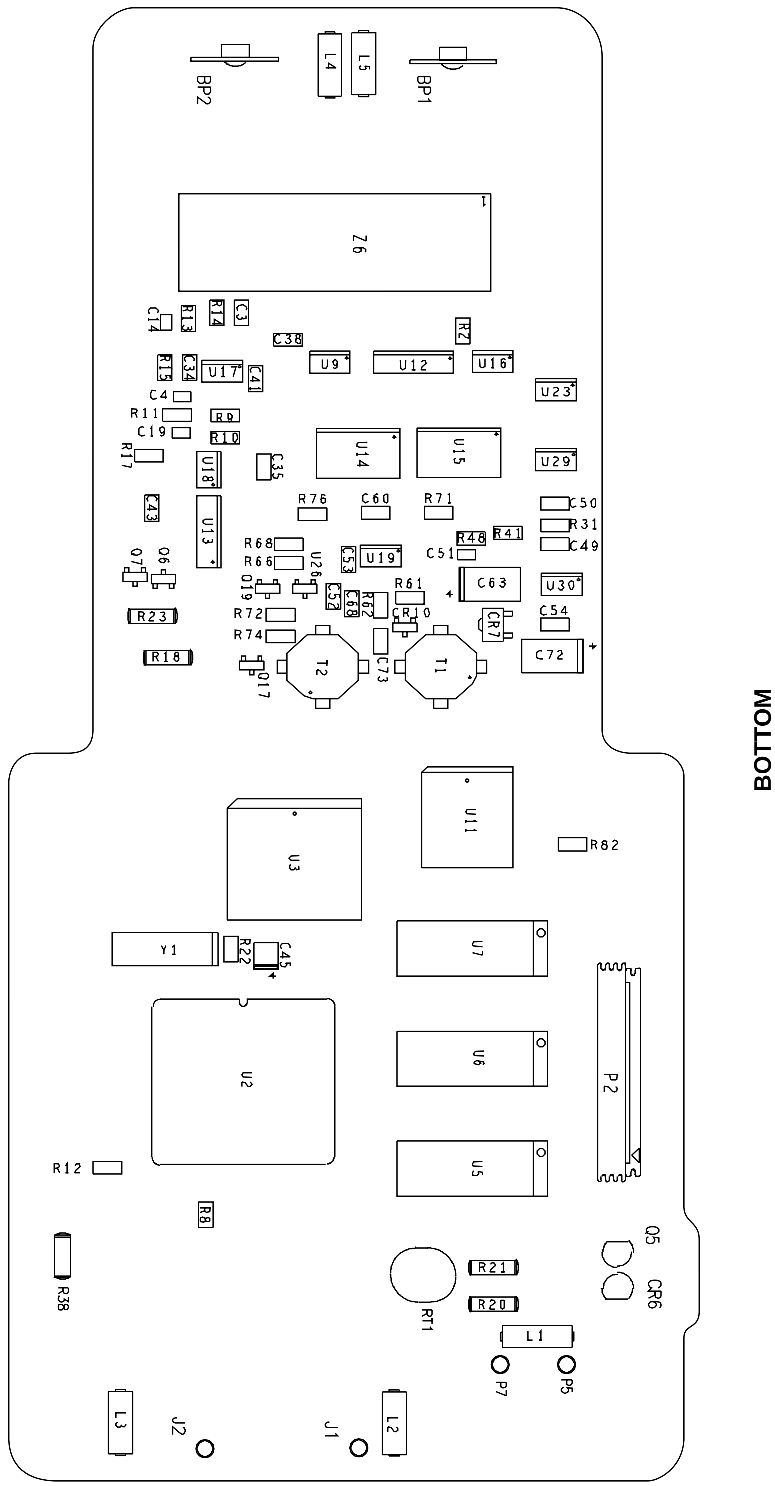
Figure 6-4. Fluke 41B A1 Main PCA



FLUKE 41B-4001
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Figure 6-4. Fluke 41B A1 Main PCA (cont)

Chapter 7
Schematic Diagrams

NOTE: 1. THE FOLLOWING PARTS ARE NOT LOADED, R73, R83, R85.

2 R33, R82, R84 AND U11 ARE LOADED FOR 41B ONLY, SEE SHEET 2.

3. UNLESS OTHERWISE INDICATED RESISTANCE IS IN OHMS.

4. UNLESS OTHERWISE INDICATED CAPACITANCE IS IN UF.

5. SHEET 6, KEYPAD, FOR REFERENCE ONLY.

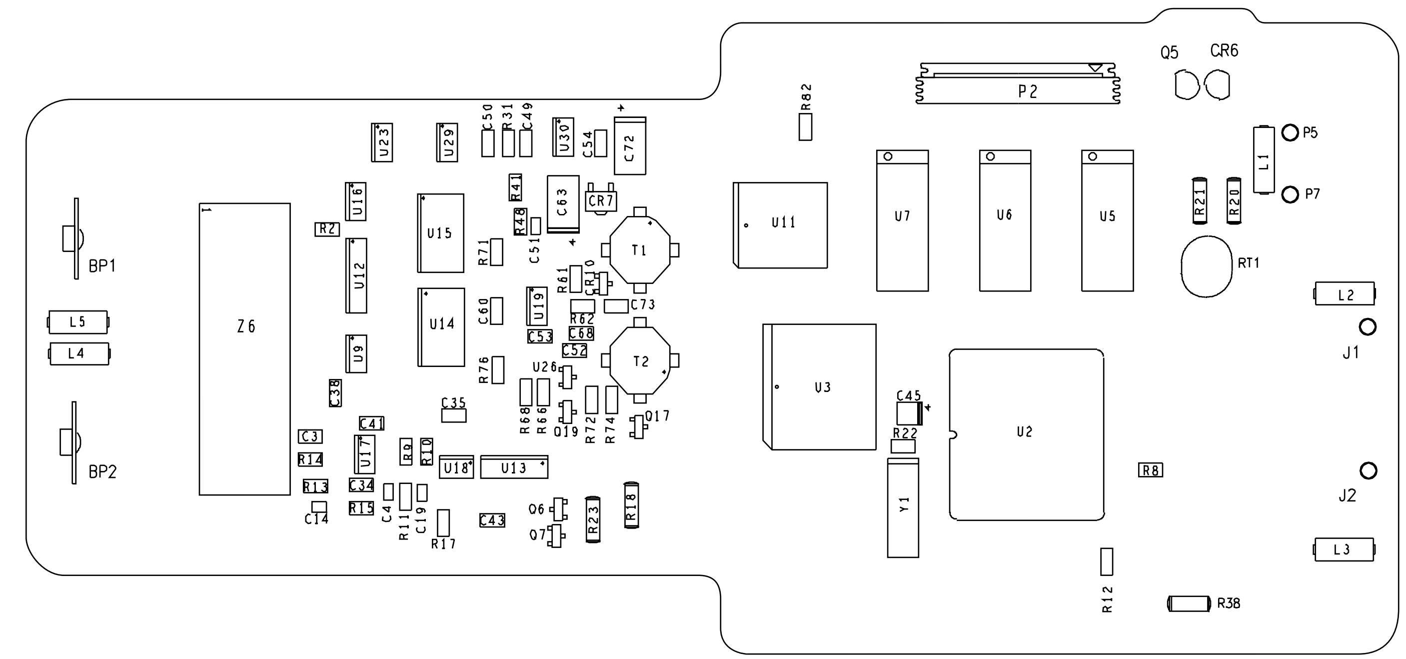
6. FOR ASSEMBLY AND REFERENCE DESIGNATION DRAWING SEE FLUKE 39 & 41B-4001 DRAWINGS.

8 R28 IS LOADED FOR BOTH THE 39 AND 41B, SEE SHEET 3.

9 R56, R39, Q21, R36, CR6, C11, Q5, R32, C12, U20, Q1, R25, C10, R29, CR1 ARE LOADED ON THE FLUKE 41B ONLY, SEE SHEET 3.

REFERENCE DESIGNATION		
	LAST USED	NOT USED
BT		
C	75	
CR	10	
F		
J	2	
P	7	
Q	21	
R	88	R78, R79
RT	1	
RV		
S		
TP		
U	31	U27
VR	1	
Y	1	
Z	8	
BP	2	
L	5	

FLUKE 4X-1021
(1 OF 6)



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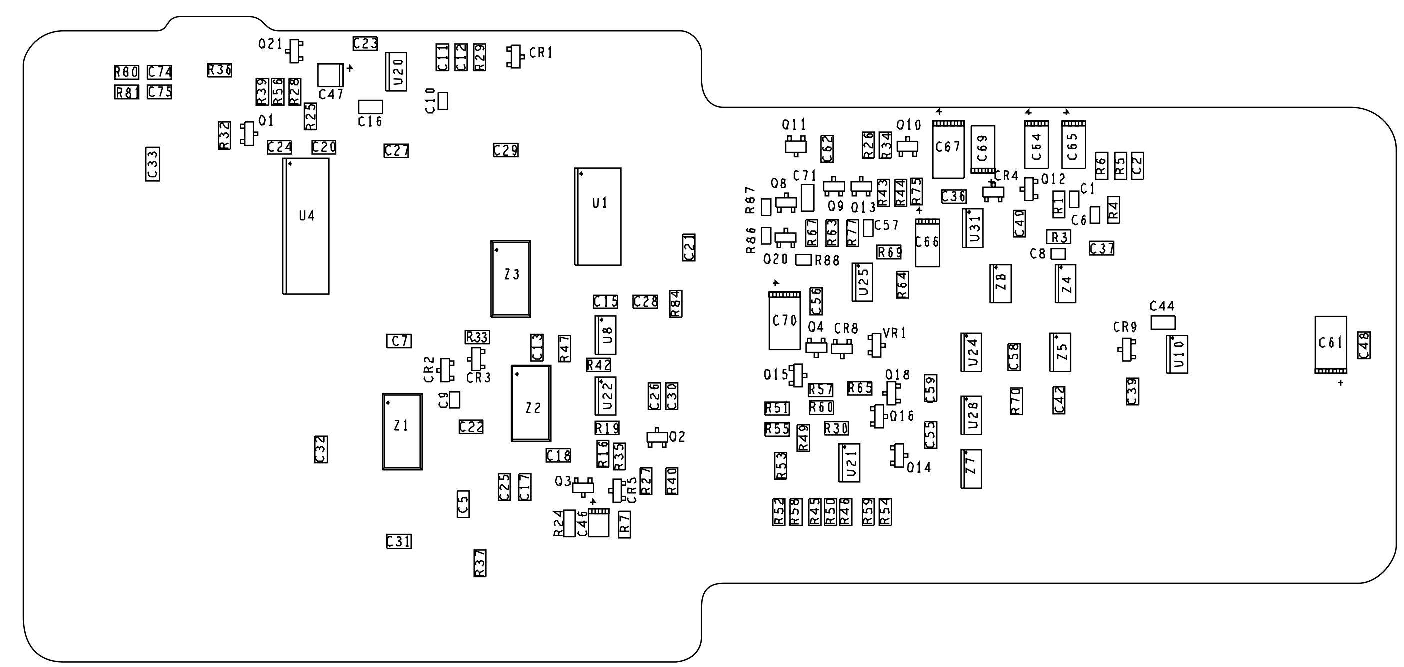

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FLUKE 41B-4001

Figure 7-1. A1 Main PCA (Fluke 39 and 41B)

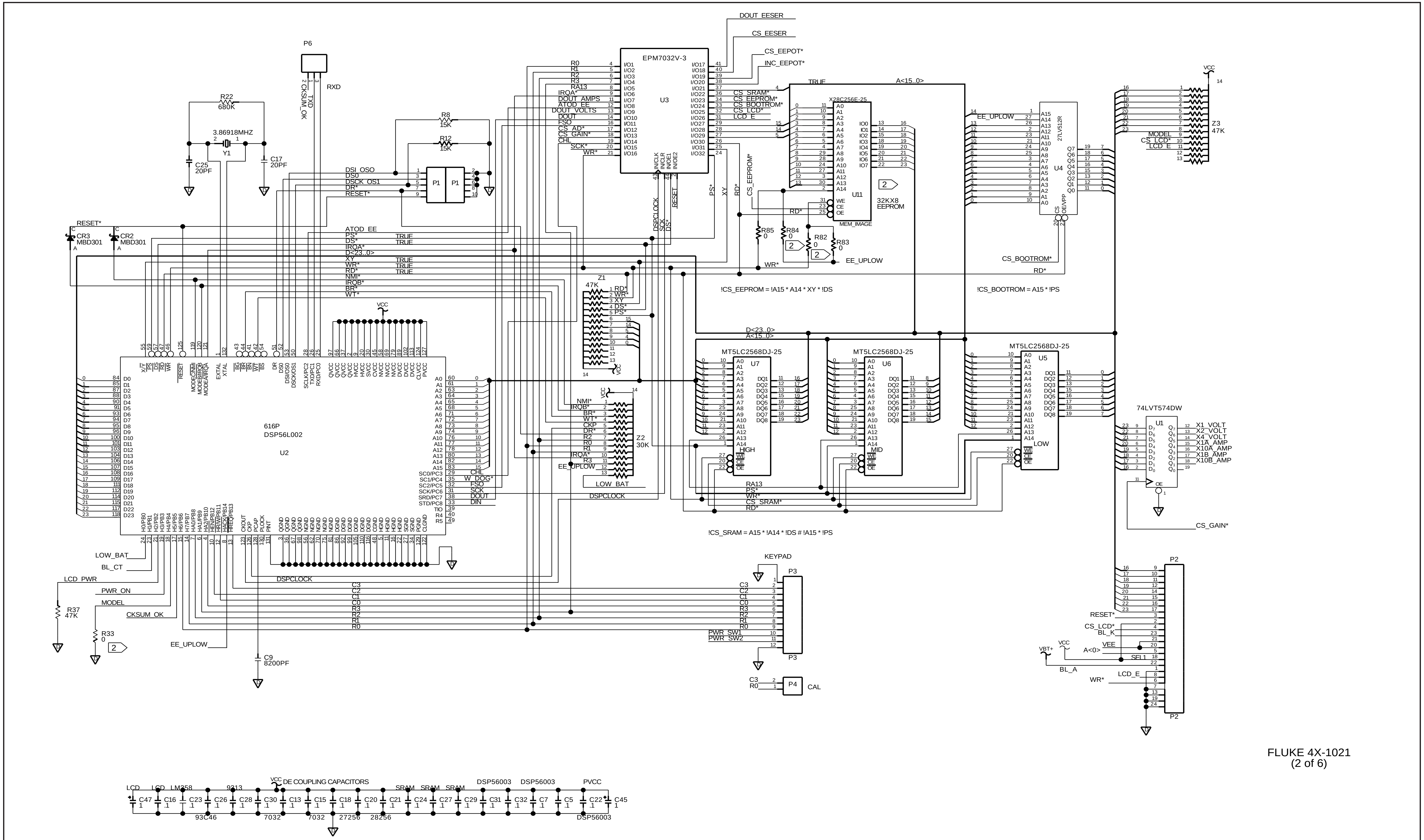

Figure 7-1. A1 Main PCA (Fluke 39 and 41B) (cont)

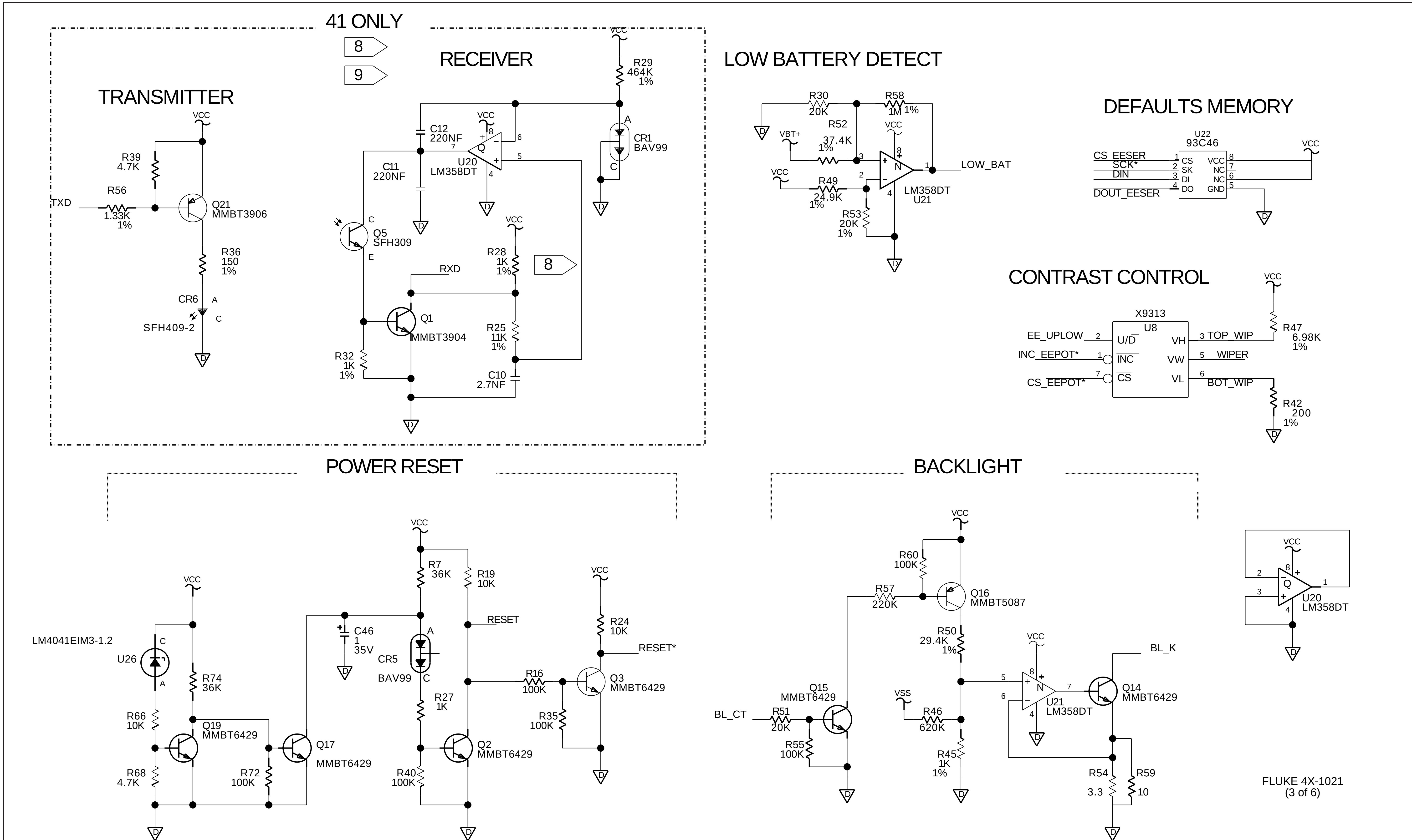

Figure 7-1. A1 Main PCA (Fluke 39 and 41B) (cont)

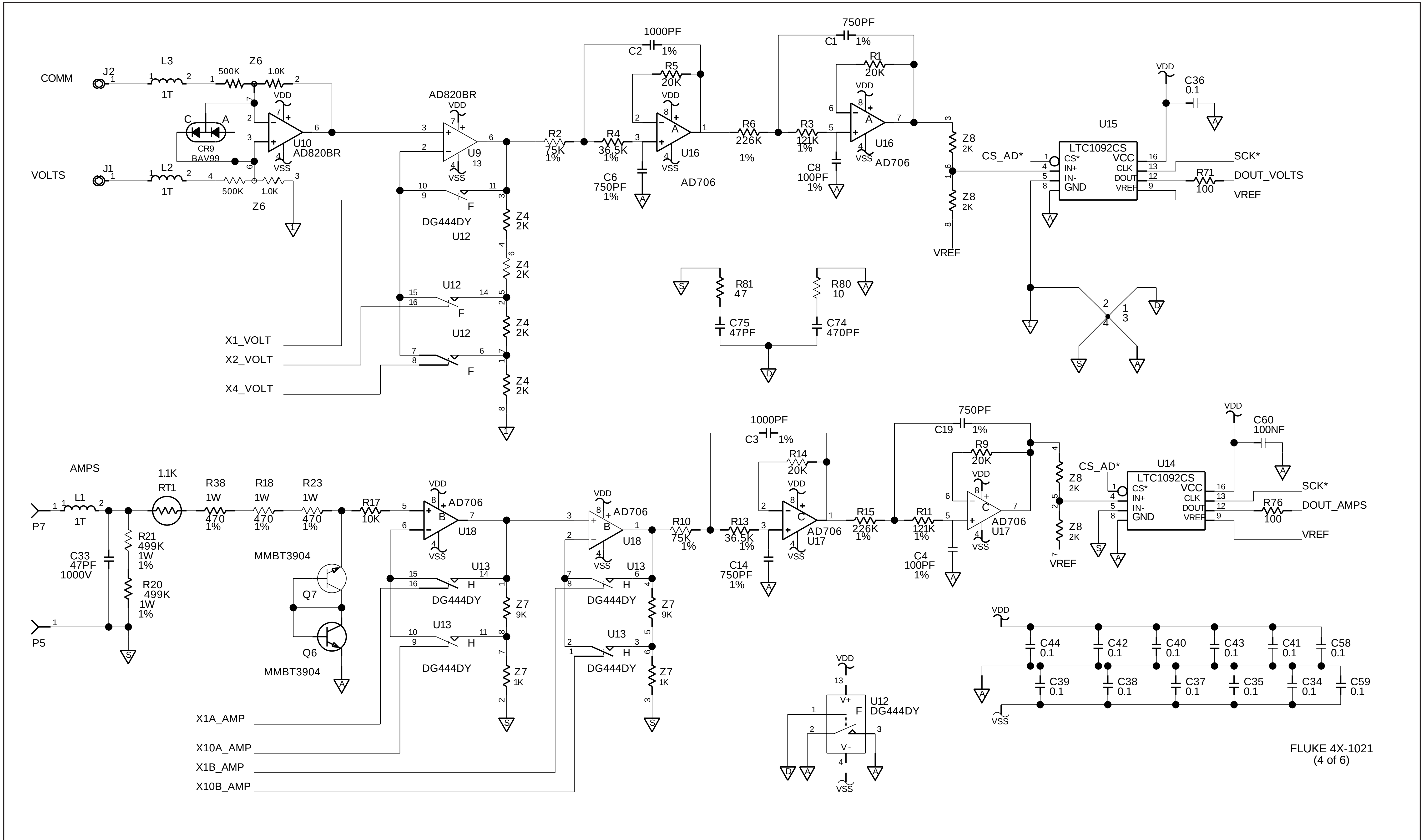

Figure 7-1. A1 Main PCA (Fluke 39 and 41B) (cont)

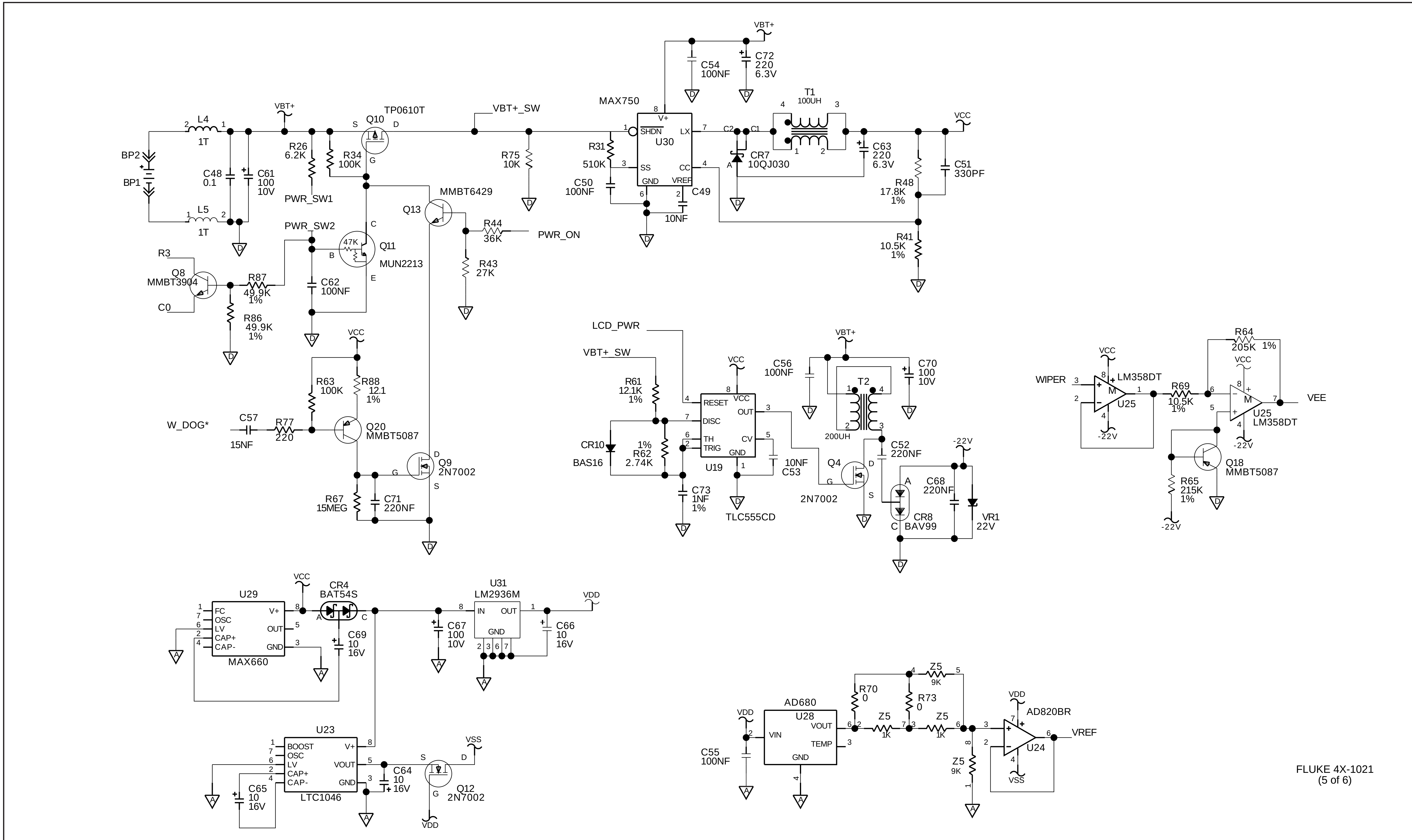

Figure 7-1. A1 Main PCA (Fluke 39 and 41B) (cont)

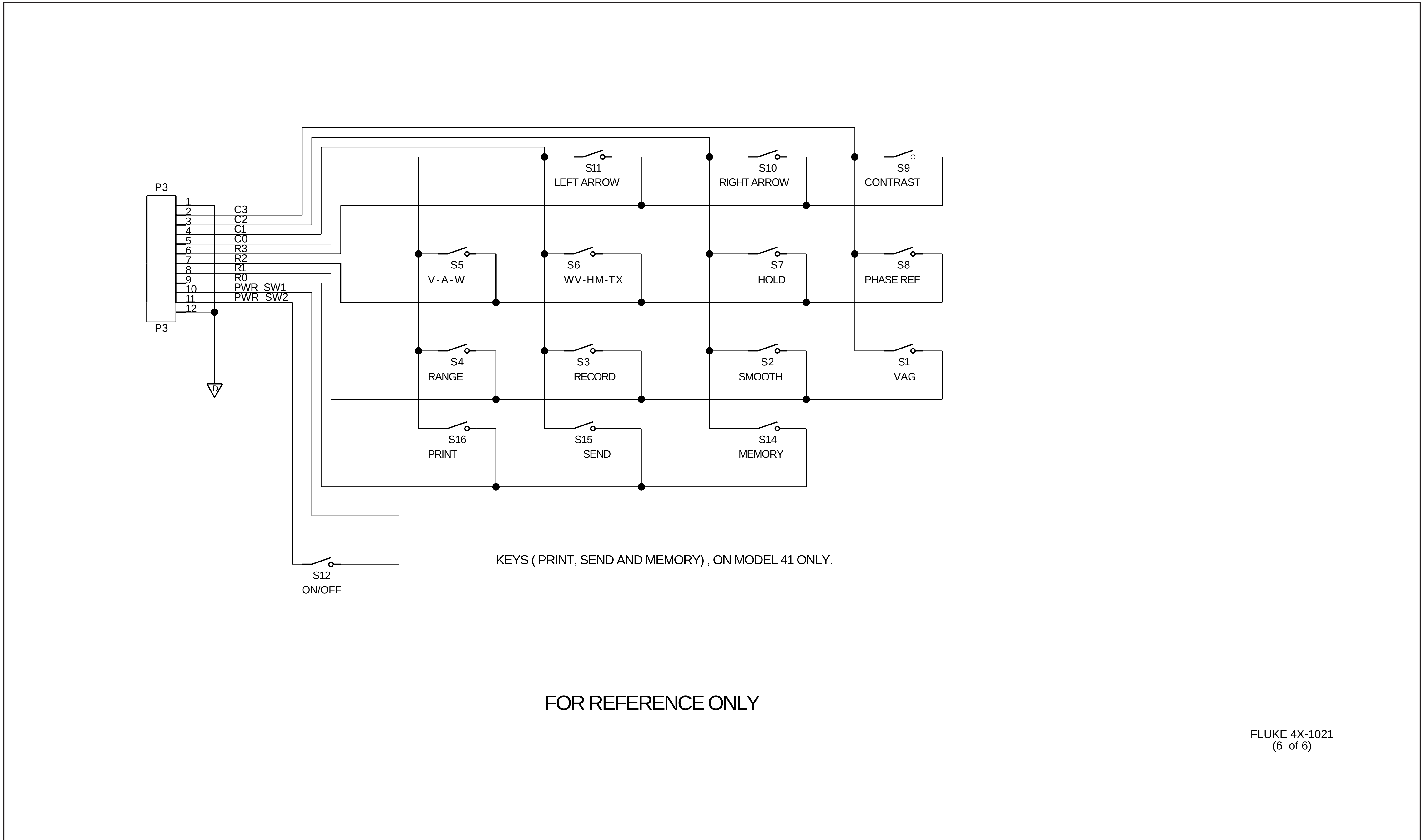

Figure 7-1. A1 Main PCA (Fluke 39 and 41B) (cont)